Virtuoso 23.1
Module 2 – Schematic View, Symbol View, and Test Bench

American University of Beirut (AUB)
Lebanon

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Module Objective

In this module, we will learn how to:

- characterize (i.e., find the basic parameters) of NMOS and PMOS transistors
- design a full circuit consisting of a common source amplifier with its biasing current source implemented as a current mirror. In our case, the specifications, which are typically handed over by the system/block-level designers, are as follows:
  - Power supply voltage: 1.1 V
  - Load = 100 kΩ
  - Voltage Gain ≥ 7.5 dB
  - Bandwidth ≥ 4 GHz
  - Average Power Consumption ≤ 2.75 mW → Average Current Consumption ≤ 2.5 mA
  - Temperature range: 10°C to 75°C
- create a symbol for our circuit
- create a testbench for our circuit to run Transient, DC, and AC simulations

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1. Creating a Library

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Some Important notes before starting

- Wire names, pin names, and variable names should be unique, which means that each identifier used within the design environment must be distinct and not duplicated.
- Cadence is case sensitive.
- Spaces and special characters shouldn’t be used when naming libraries, variables, pins, or wires.

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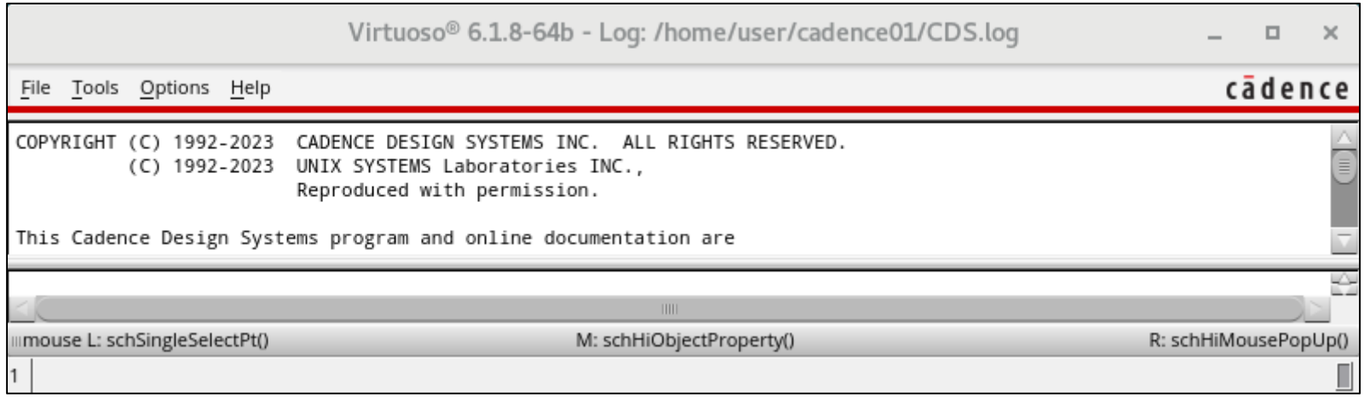
Symbol
Test Bench

1. Creating a Library

- Launch Virtuoso.
- Below is the Command Interpreter Window (CIW), this is the main window. The tool outputs all the messages that it needs to communicate with us.



- Sometimes a window opens behind the one where you are currently working. Make sure to check the taskbar for new files.
- If a message regarding the license pops up, click on **Always.**

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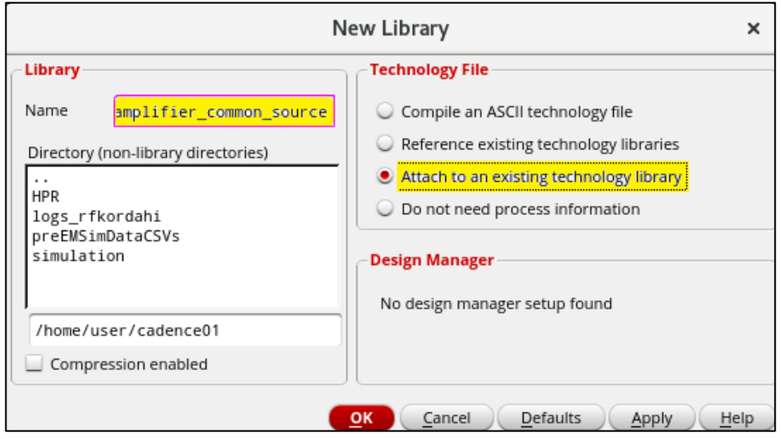
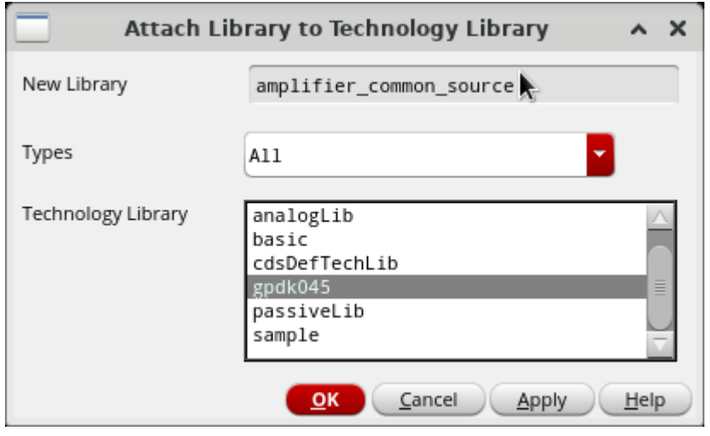
1. Creating a Library *(continued)*

- Select **File → New → Library…**
- Enter a name for the **Library.** In this module, we will name it "**amplifier_common_source**".
- In our library, we are going to include real components that came in the design kit. Therefore, we attach the technology file (which is a specific library) to our library.
- We will be using the 45nm CMOS process.
- The name of the library is **gpdk045** where "pdk" stands for "process design kit".
- This library contains the real components that are fabricated as part of the integrated circuit.
- Click on "Attach to an existing technology library", add the "gpdk045", and click OK.





- You should not give a library the name of an existing one because it will overwrite it.
- The documentation of this pdk can be accessed from the Linux desktop.
- Cadence is case sensitive, and spaces and special characters are not allowed when naming a library

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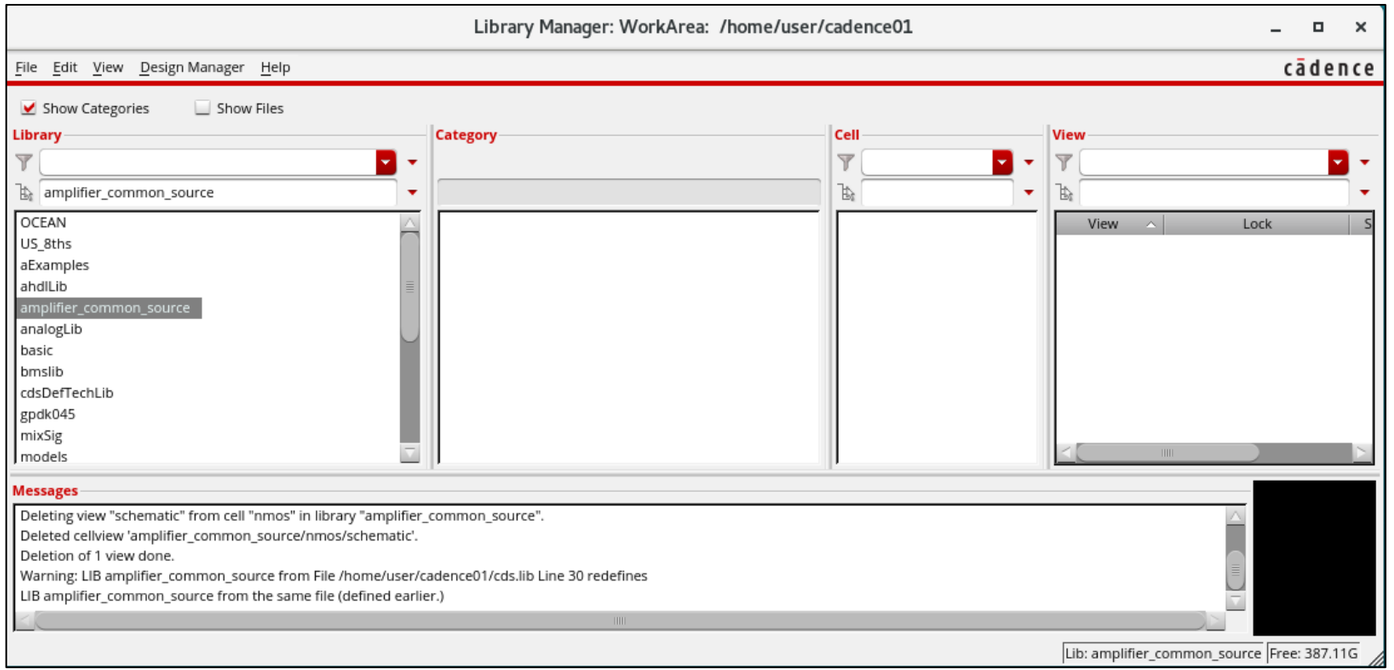
1. Creating a Library *(continued)*

- Select **Tools → Library Manager…**
- Here you can find all your libraries as well as the built-in libraries and their contents.



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Useful Bindkeys (Shortcuts) in Schematic Editor

Combination	Action
I	Create Instance
P	Create Connection
Ctrl + P	Create Pin
L	Create Connection Name
Ctrl + X	Descend Read
J	Rotate
C	Copy
M	Move
U	Undo
Shift + U	Redo
F	Zoom to Absolute Scale
[	Zoom Out
]	Zoom In
Q	Edit Object Properties
Ctrl + A	Select All
Ctrl + D	Deselect All
F8	Check and Save
F1	Cadence Help

- To get all the Bindkeys, in CIW (main Cadence window): Options → Bindkeys…

- Note that the Bindkeys depend on the exact tool setup.
- The shortcuts are usually indicated next to the command in the menu.

Implementing Units Prefixes with Corresponding Letters

Prefix		Corresponding letter
Giga	10^{9}	G
Mega	10^{6}	M
Kilo	10^{3}	k
milli	10^{-3}	m
micro	10^{-6}	u
nano	10^{-9}	n
pico	10^{-12}	p
femto	10^{-15}	f

- Note that no spacing should be between the last digit and the unit prefix.

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2. Drawing the Schematics

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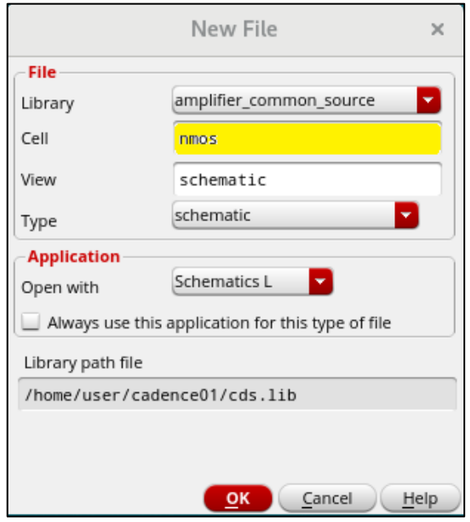
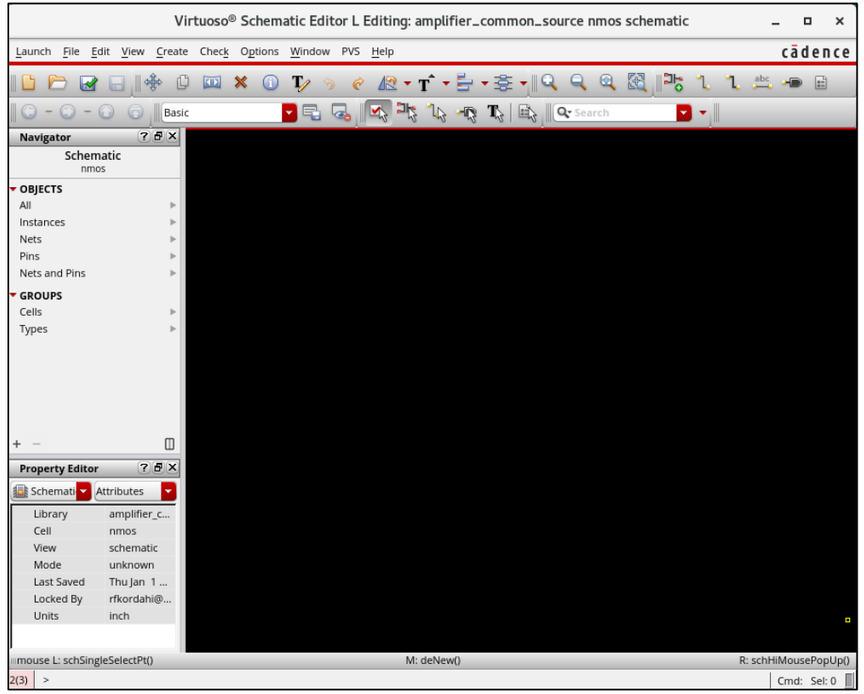
2.a. NMOS

- From the Library Manager, select your library.
- Select **File → New → Cell View**.
- Name the Cell "**nmos**" and click **OK** (make sure both fields Library and Type are set as shown below).
- The Schematic Editor pops up.
- This is where we will create our circuit.





- Note that the editor window can take some time to pop up or can even pop up in the background. Make sure to check the taskbar.

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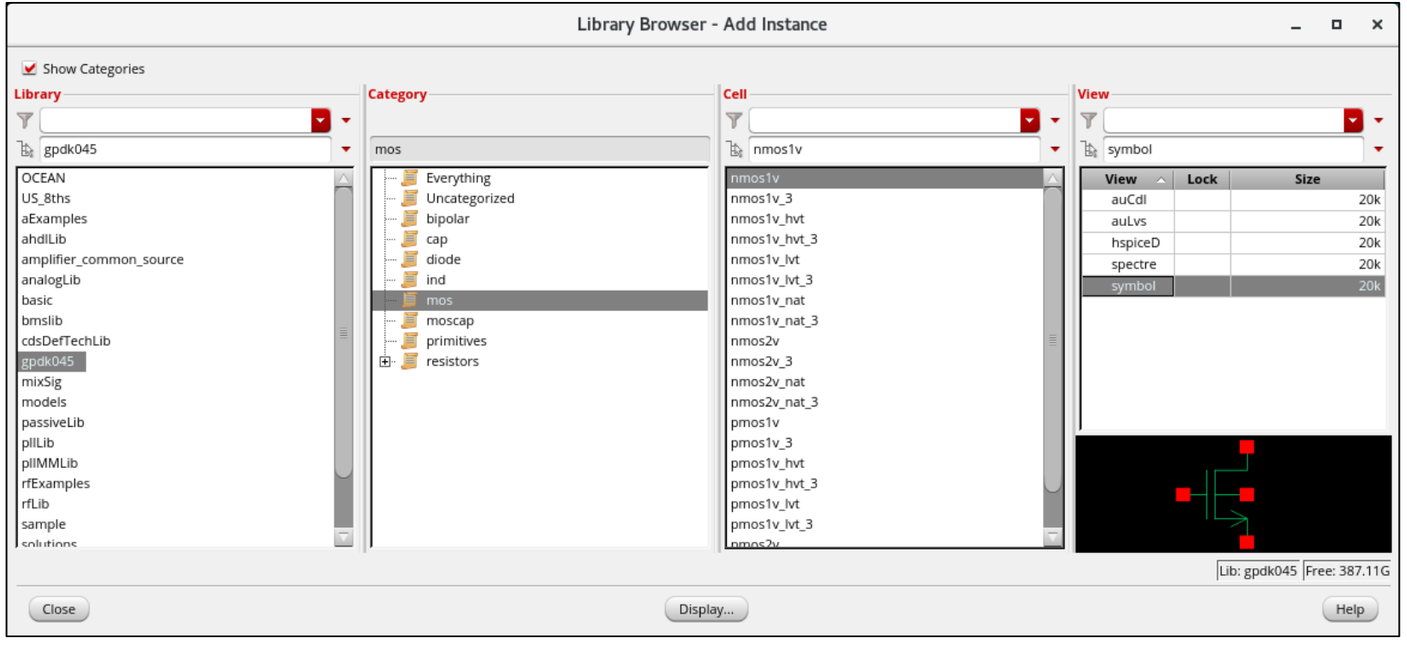
2.a. NMOS *(continued)*

- From the Schematic Editor, select **Create → Instance → Browse**.
- Select the NMOS transistor from the gpdk045 library as shown below.



- Note that next to every command there is a keyboard shortcut you can use, which eases the work.

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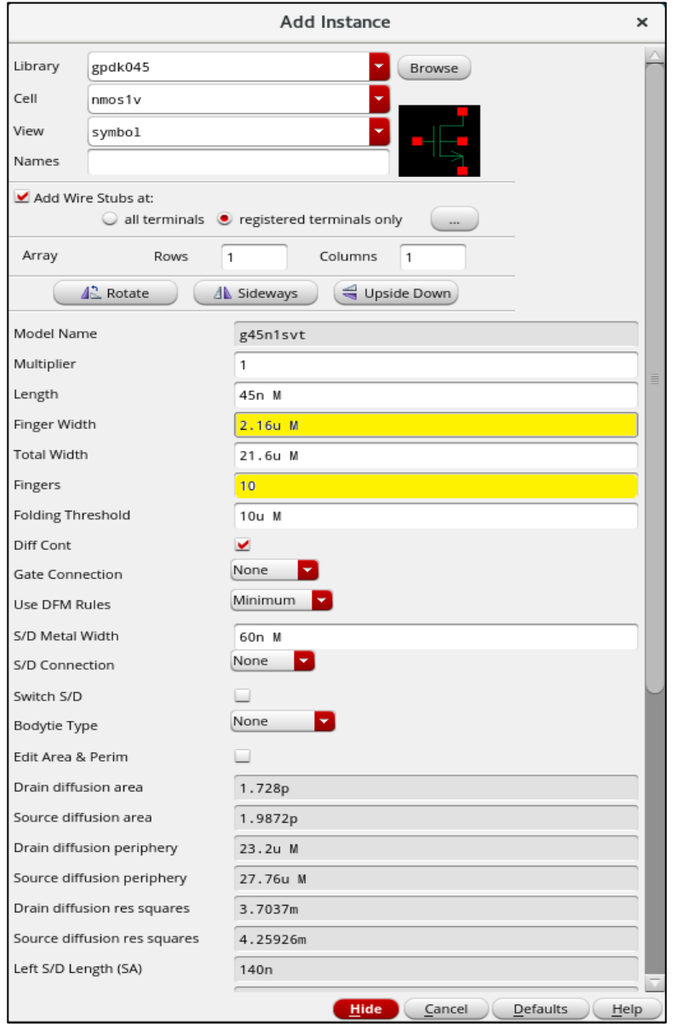
2.a. NMOS *(continued)*

- Place the transistor in the Schematic Editor.
- Select the transistor, then **right-click** and select **properties…**
- Here you can change the different parameters of the transistor.
- First, set the **Fingers** to **10**, and then set the **Finger Width** to **2.16µ**.



- For every parameter, you can set its visibility using the drop-down menu to its right.
- Keep in mind that there should be no gap between the last digit and the metric unit when inserting it (2.16u in this case).

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2.b. NMOS *(continued)*

- It's worth noting that if the instance isn't visible in the schematic, it's because the instance's image, as shown in the figure below, isn't visible.
- Make sure that the NMOS transistor is shown in the image next to the view option.
- You can make the image appear by selecting "symbol" from the view option's drop-down menu.

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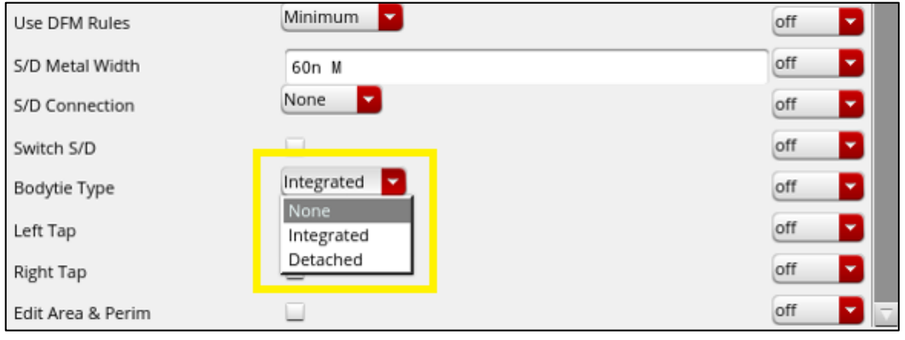
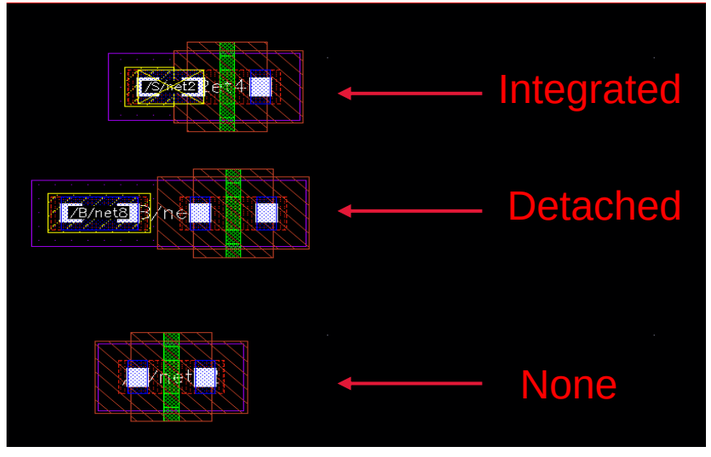
2.b. NMOS *(continued)*

- One additional feature in the transistor's attributes include a parameter called Bodytie Type, which allows us to select between three different types: **None**, **Inherent**, and **Detached**.
  - **None**: Transistors may be designed with their body terminals floating or with the assumption that they are linked to the substrate.
  - **Integrated**: Transistors automatically connect their body terminals to an initial or specified voltage.
  - **Detached**: Transistors' body terminals or disconnected from any particular voltage source or node.
- In the event that the setting is "none" or "detached," manual intervention may be necessary during layout to ensure that NMOS and PMOS transistors are properly bodytied to the right voltage sources or nodes.





- Please take note that this slide is for educational purposes only.
- For the purposes of this project, the transistor's body will be connected to the source terminal with the body tie set to **none**, which means we will set up the body tap ring manually.

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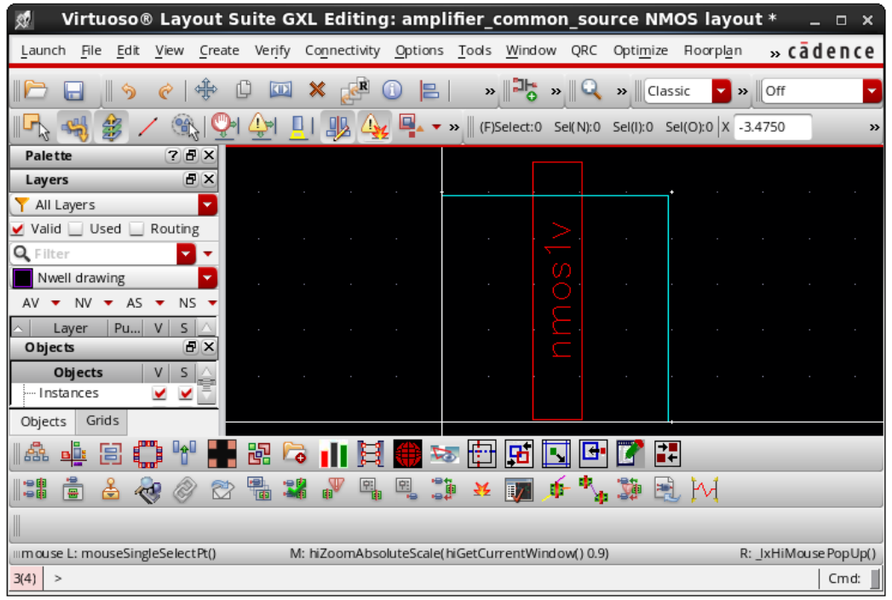
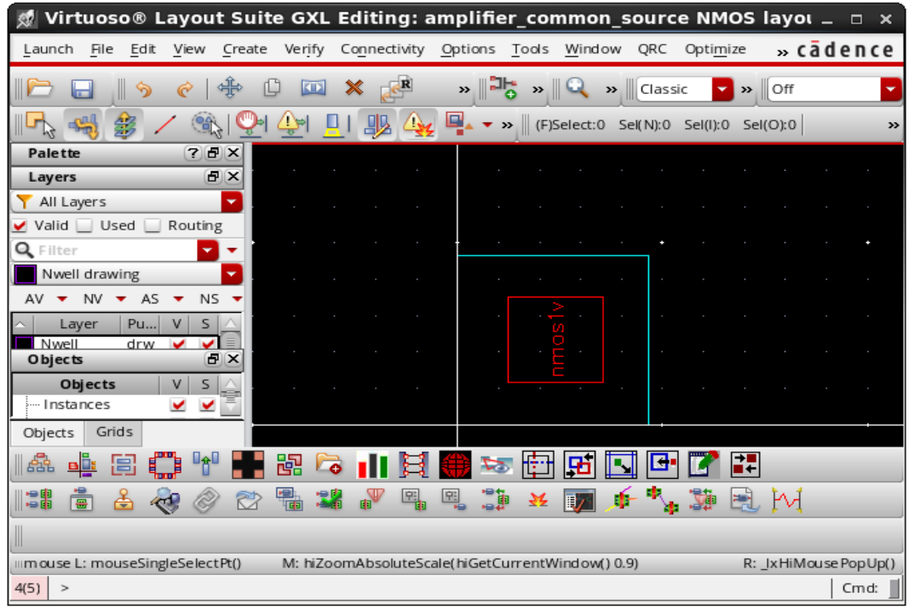
2.a. NMOS *(continued)*

- Below is the difference between a transistor having 3 fingers (left figure) and 10 fingers (right figure), both with the same total width (21.6 µm), as seen in the Layout GXL tool which we will use in Module 8.





- The result of having multiple transistors in parallel or multiple fingers will change the shape of the transistor in the layout tool.

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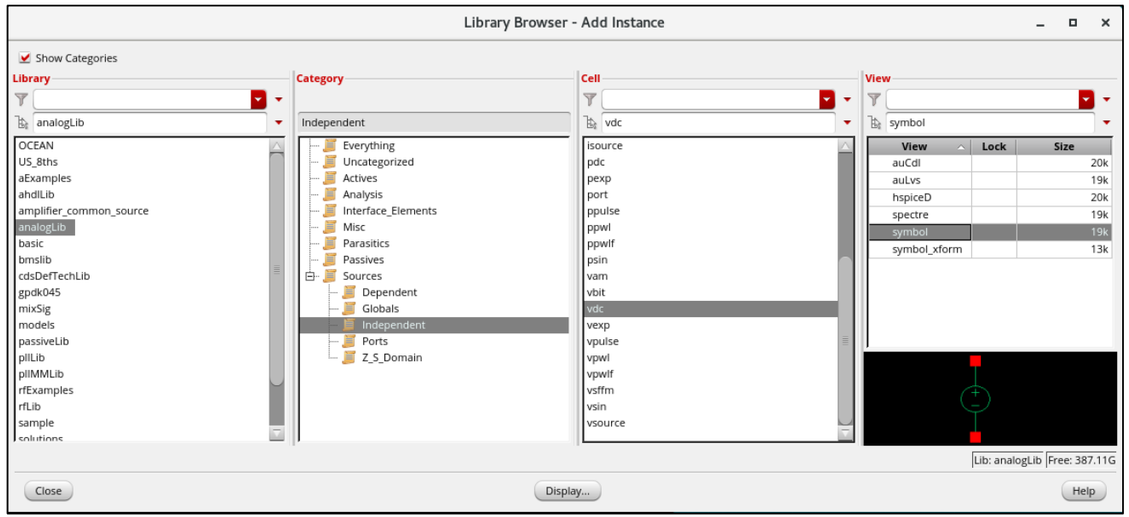
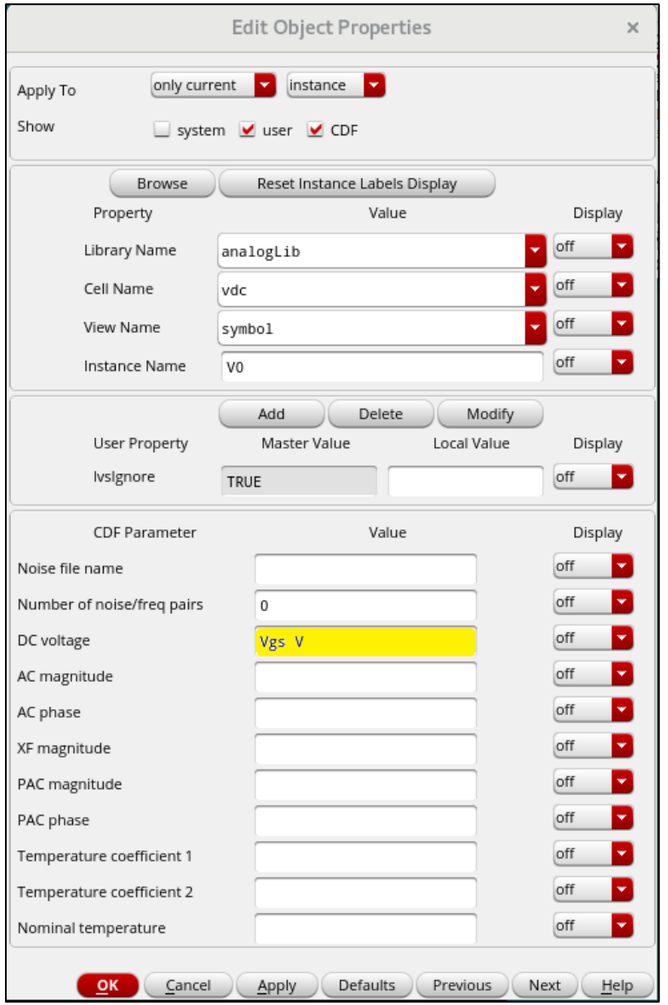
2.a. NMOS *(continued)*

- Insert **two independent dc voltage sources** from the library **analogLib**.
- The analogLib library contains ideal components.
- Set the DC voltage value of the first source to **Vgs**.
- Set the DC voltage value of the second source to **Vds**.





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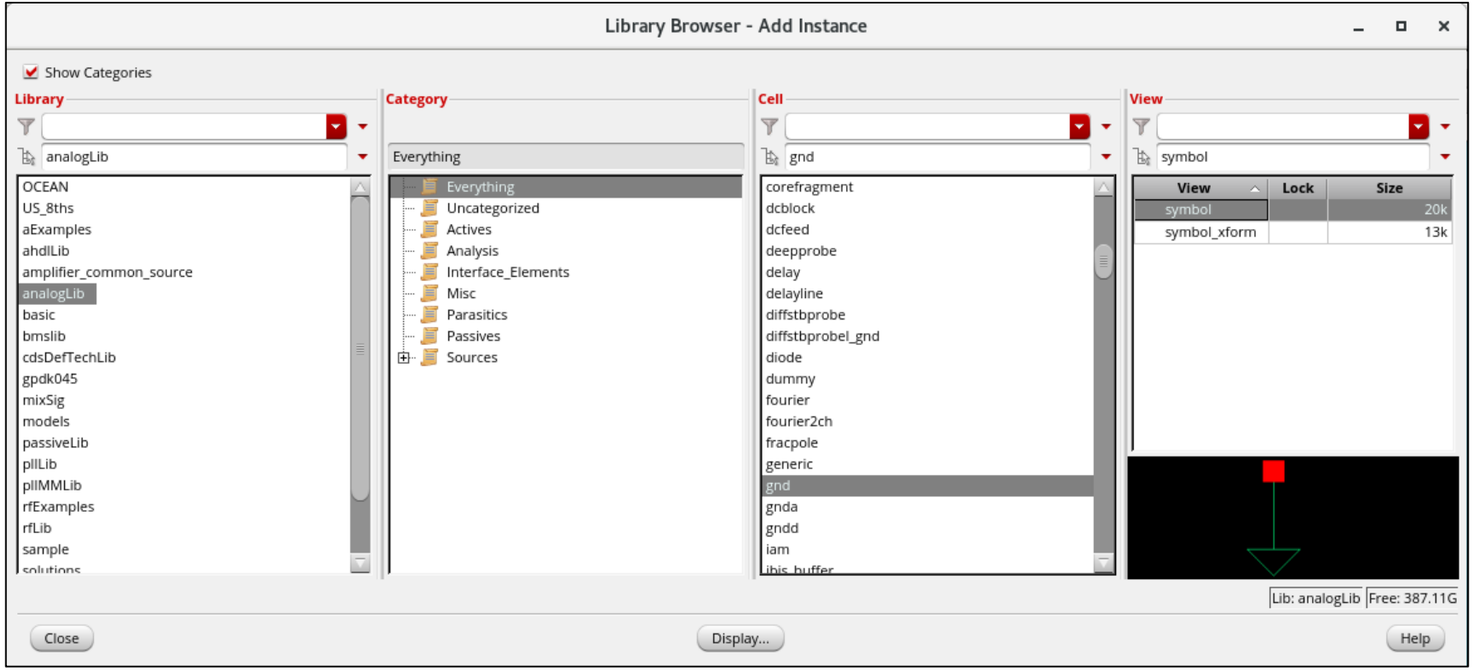
2.a. NMOS *(continued)*

- Add a ground from the analogLib library as shown below.
- At any time, you can cancel a command by pressing the **Esc** key.



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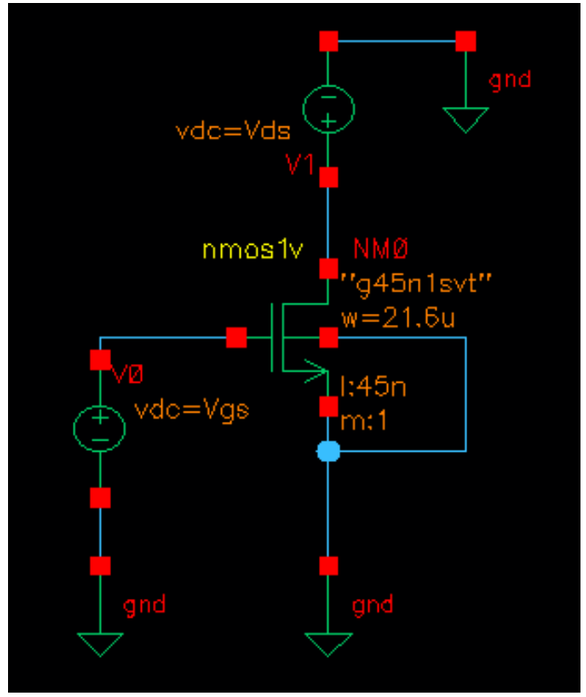
2.a. NMOS *(continued)*

- Select **Create → Wire**, or press **p**.
- Connect the components.
- Flip the Vds voltage source by right clicking on it and choosing rotate. Rotate twice to obtain as shown in the figure.
- Complete the circuit as shown.
- You now have a circuit of an **NMOS**, connected to **Vds** and **Vgs**.



- Note that in case the designer wants to add a bulk connection, the bodytie type in the properties of the NMOS should be checked.

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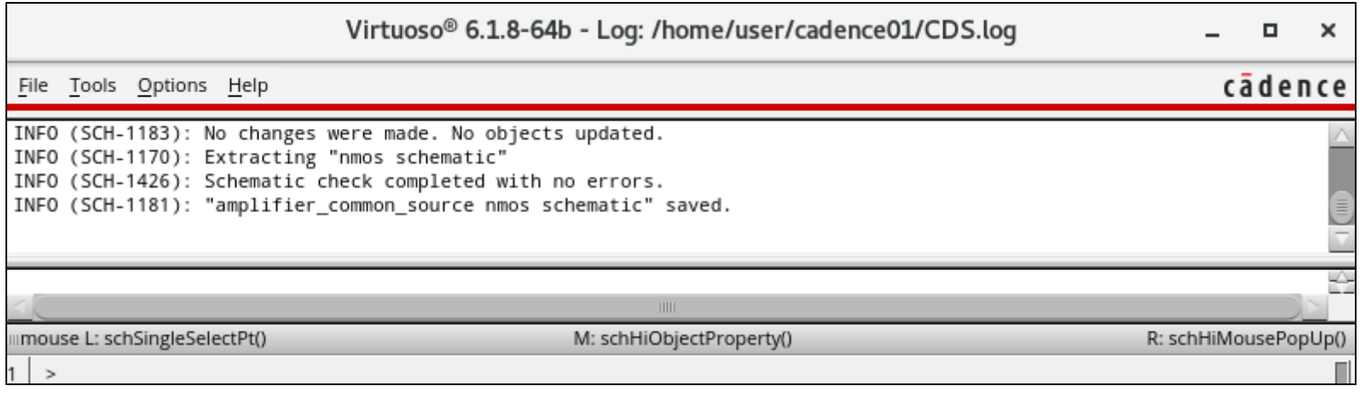
2.a. NMOS *(continued)*

- Select **File → Check and Save**.
- If there is an error, a message will be shown in the **CIW** window, otherwise the CIW outputs the messages below.



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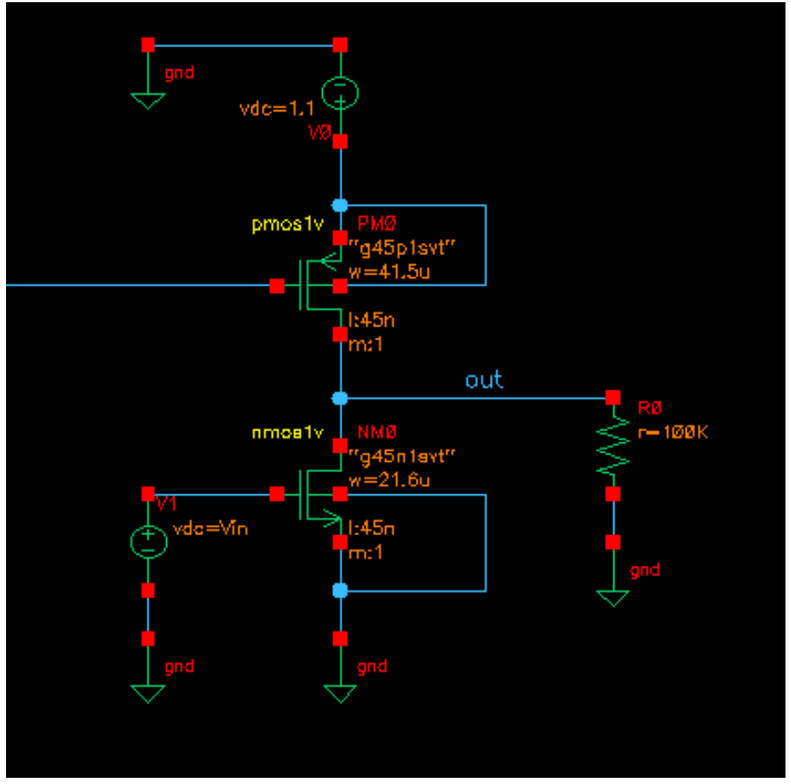
2.a. NMOS *(continued)*

- For the “nmos1v” transistor, the threshold voltage is around 600 mV, therefore we choose a value higher than 600 mV for Vgs. In our example, we will choose 650 mV.
- Note that later when we design the common source amplifier, the values of the parameters will be the same. As you can see in the figure, there will be a PMOS above the NMOS, and the output node is at the drain of the NMOS or the PMOS. Ideally, we would like the output to swing as much to the top as to the bottom, as a result we set the dc of the output at the middle (550mV) of Vdd. Therefore, Vds of the NMOS transistor would be 550 mV.



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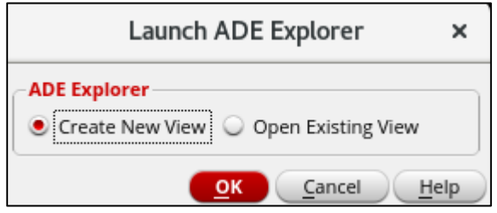
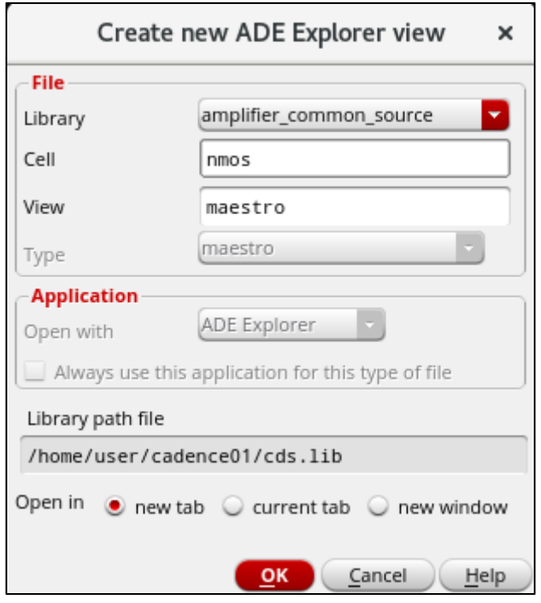
2.a. NMOS *(continued)*

- Now we will use the tool ADE Explorer to run the analyses.
- In Schematic Editor, select **Launch → ADE Explorer**.
- The window “Launch ADE Explorer” pops up. Select “Create New View” and click OK.
- Make sure the fields of the window “Create new ADE Explorer view” is as shown below.
- Click OK to proceed.





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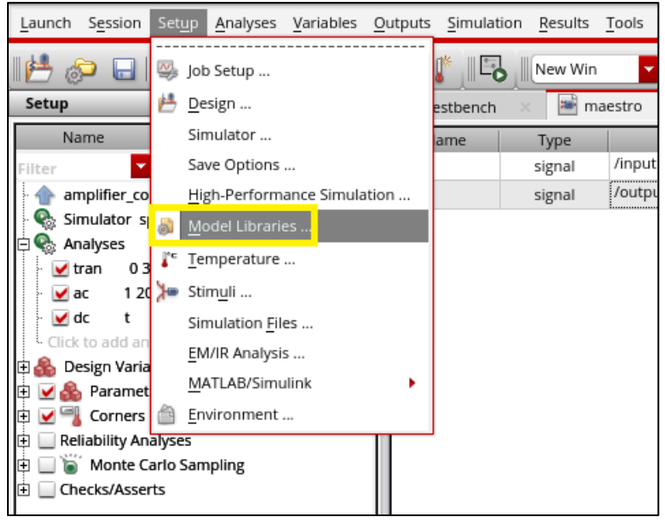
2.a. NMOS *(continued)*

- The maestro view opens.
- You still need to add the model files (these files define the parameters of the components used in your circuit, thus implicate your circuit behavior).
- Select **Setup → Model Libraries…**



- Make sure to always change the model library as tt when you open any maestro view.
- The maestro view sets by default the model libraries to mc which is not what we want.

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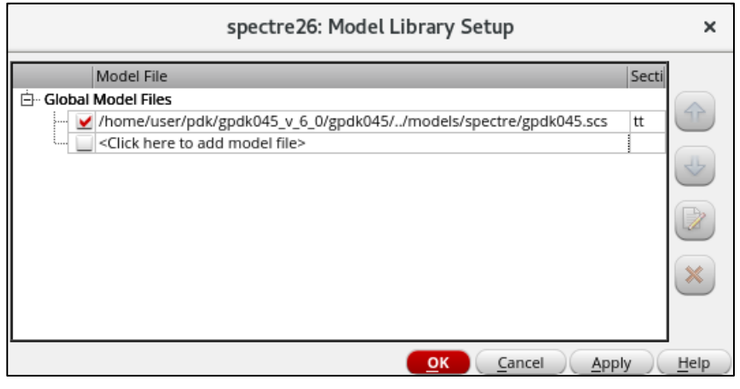
2.a. NMOS *(continued)*

- The tool may have already defined the Model Library.
- If this is the case, the file “gpdk045.scs” will be selected as shown below.
- Click on the **Section** field and **select** “tt” from the drop-down list. It stands for “Typical NMOS Typical PMOS” process conditions.
- Click **OK** to save your “Model Library Setup”.



- If the tool hasn’t defined the Model Library, the next few slides explain how to select the file “gpdk045.scs”.

- Make sure to always change the model library as tt when you open any maestro view.
- The maestro view sets by default the model libraries to mc which is not what is needed for real world applications.

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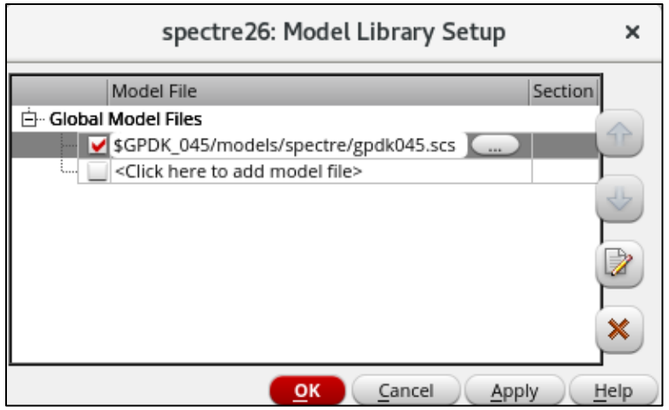
2.a. NMOS *(continued)*

- When the “Model Library Setup” form pops-up, click on <Click here to add model file>.
- **Enter** the following directory:

“*$GPDK_045/models/spectre/gpdk045.scs*”

- *Note that the “GPDK_045” must point to the root folder of the pdk, “gpdk045_v_6_0”.*



- Make sure to always change the model library as tt when you open any maestro view.
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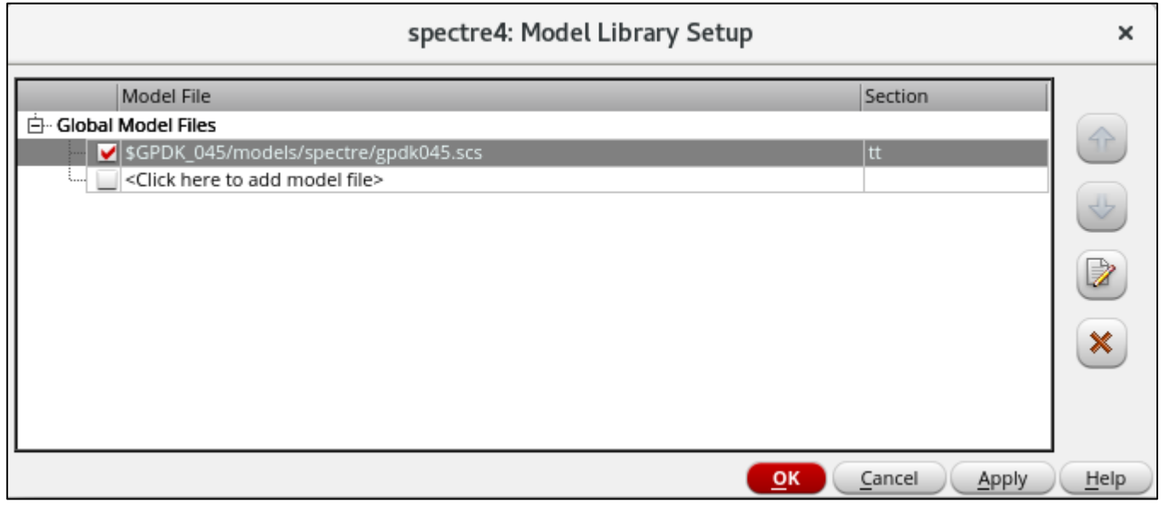
2.a. NMOS *(continued)*

- Click on the **Section** field and **select** “tt” from the drop-down list, it stands for “Typical NMOS Typical PMOS” process conditions.
- Click **OK** to save your “Model Library Setup”.



- Make sure to always change the model library as tt when you open any maestro view.
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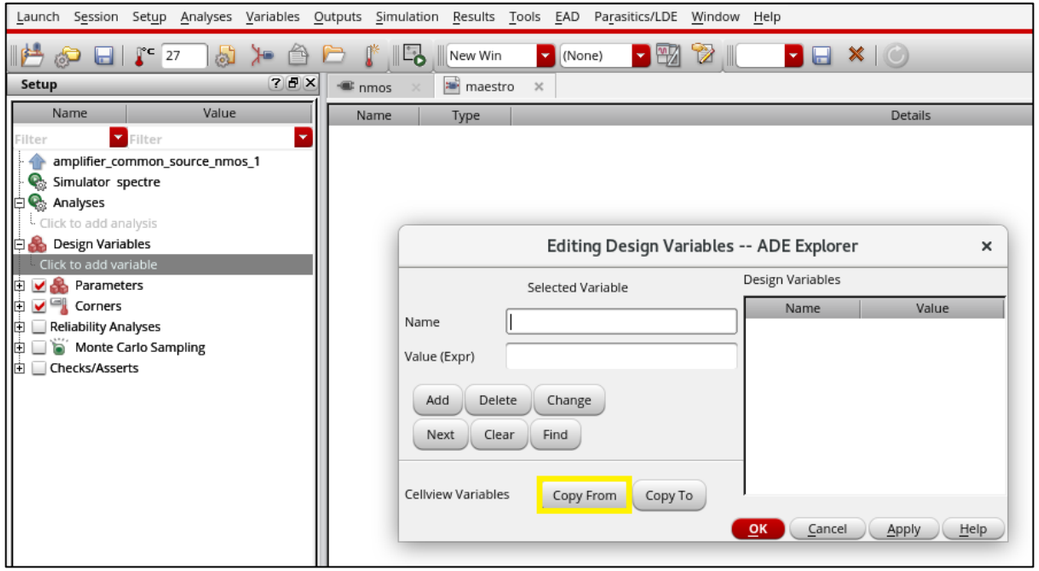
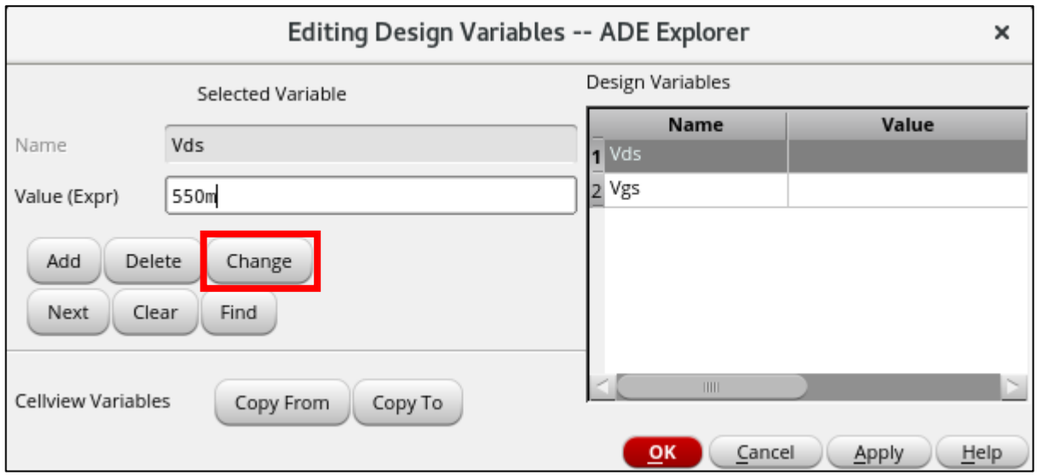
2.a. NMOS *(continued)*

- Click on “Click to add variable” under the Design Variables.
- The window “Editing Design Variables” pops-up. Select **Copy From**.
- Both Vds and Vgs will be added in the Design Variables.
- Select Vds and change the **Value (Expr)** field to 550 mV and click on **Change**.
- Select Vgs and change the **Value (Expr)** field to 650 mV and click on **Change**.
- Then click on **OK**.





- To insert the value 550 mV for Vds, in the value (expr) box 550m should be typed in only.
- Make sure to not leave any spacing between the last digit and the metric unit.

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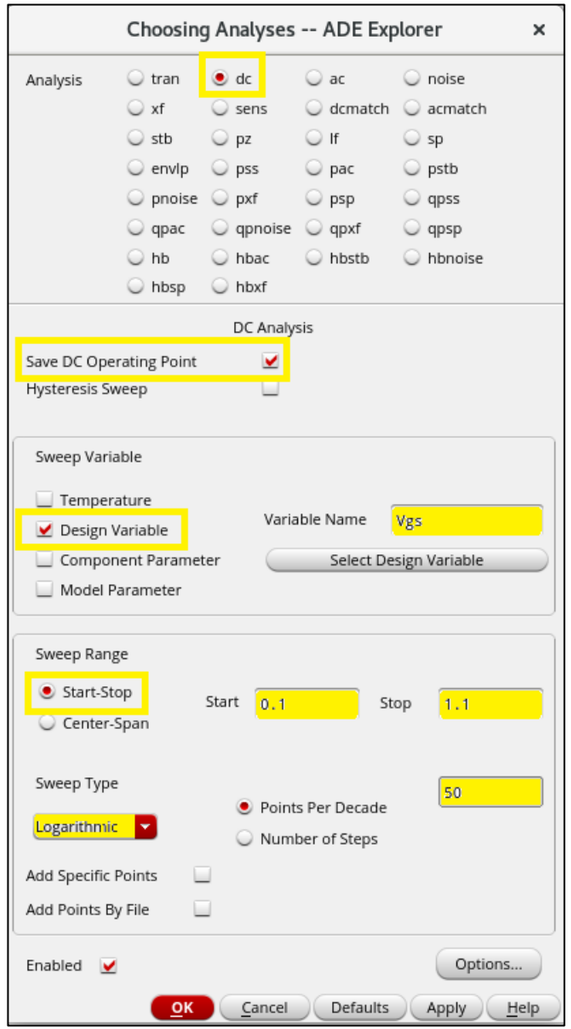
2.a. NMOS *(continued)*

- To run a simulation, we need to choose the type of analysis. Select **Analyses → Choose…**
- **tran** is the regular time-domain simulation.
- Select **dc**.
- Check the “Save DC Operating Point” and check the “Design Variable” under the Sweep Variable.
- In the **Variable Name** field type **Vgs**.
- The **Start** point should be 0.1 and the **Stop** should be 1.1.
- The maximum voltage that can be across the nmos is 1.1V.
- Select the Sweep Type as **Logarithmic** and set the Points Per Decade to **50**.
- Click OK to add the analysis.



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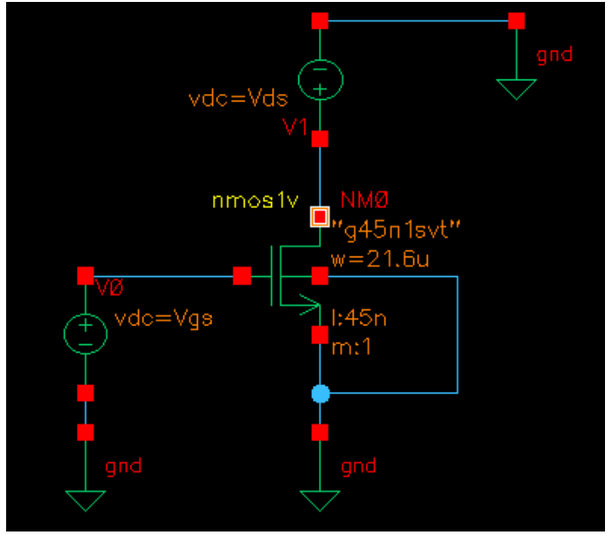
2.a. NMOS *(continued)*

- Select **Outputs → To Be Plotted → Select on Design**.
- By clicking on a connection, we select the voltage.
- By clicking on a device terminal (red square), we select the current going into the device. We want to plot the drain current, so we click once on the red square at the drain of the transistor.
- If you have done any changes to the circuit, make sure to check and save in the Schematic Editor.



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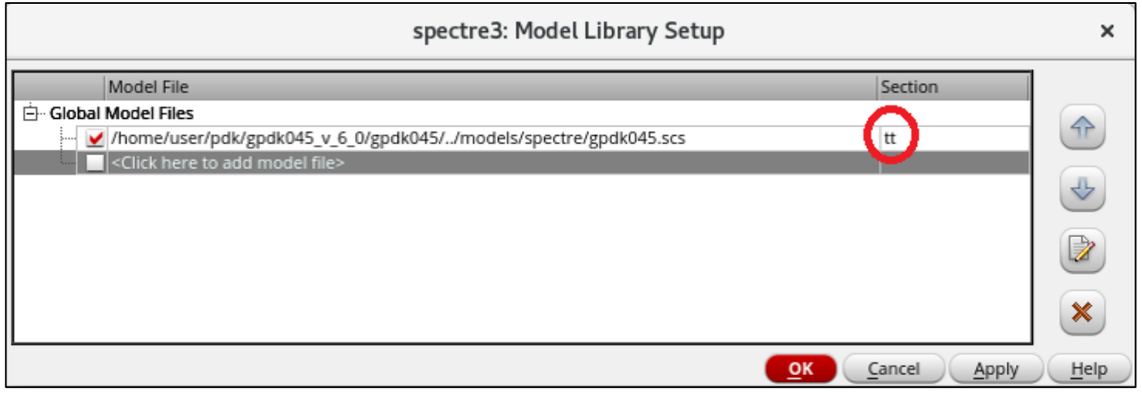
2.a. NMOS *(continued)*

- In the maestro view, the output expression is added after selecting the red terminal.
- The process condition (section) used for the simulations is “mc”. It should be changed to “tt”.
- From Setup → Model Libraries, change the section to “tt”.



cadence

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- Library
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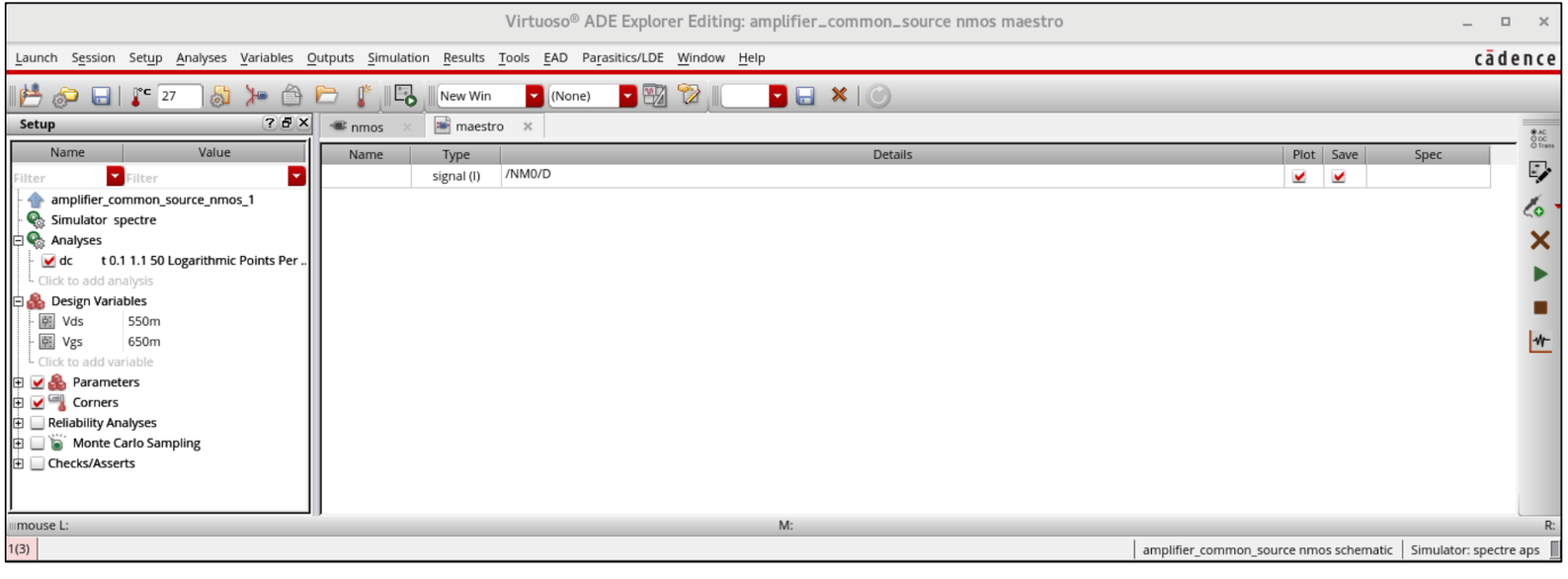
- PMOS
- CS Amplifier
- Symbol
- Test Bench

2.a. NMOS *(continued)*

- Save the session by selecting **Session → Save**.
- To run the simulation, select **Simulation → Netlist and Run** or simply click on the **Run Simulation** button (green button) on the right side of the Explorer window.
- A window will pop-up, showing what the simulator is doing.
- If there are no errors, the tool VIVA XL (Virtuoso Visualization & Analysis XL) plots the output expression.



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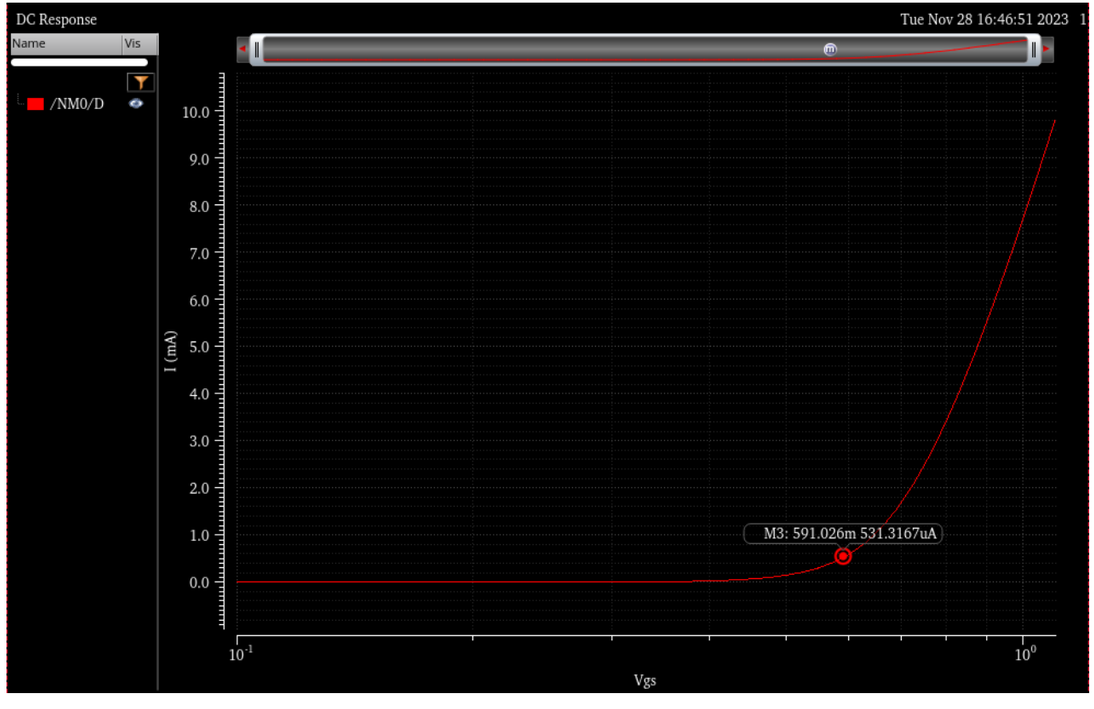
2.a. NMOS *(continued)*

- To create a marker, select **Marker → Create Marker…**
- Select “Point” and place it where the slope starts to increase.
- This is the Threshold Voltage Vth (591 mV).



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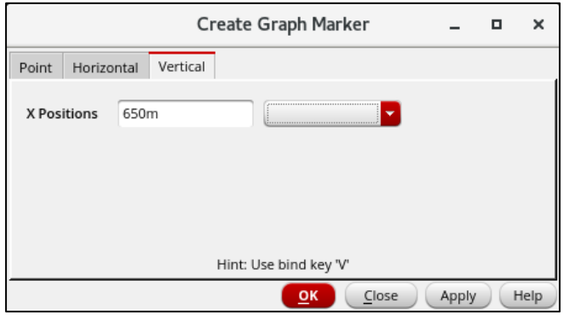
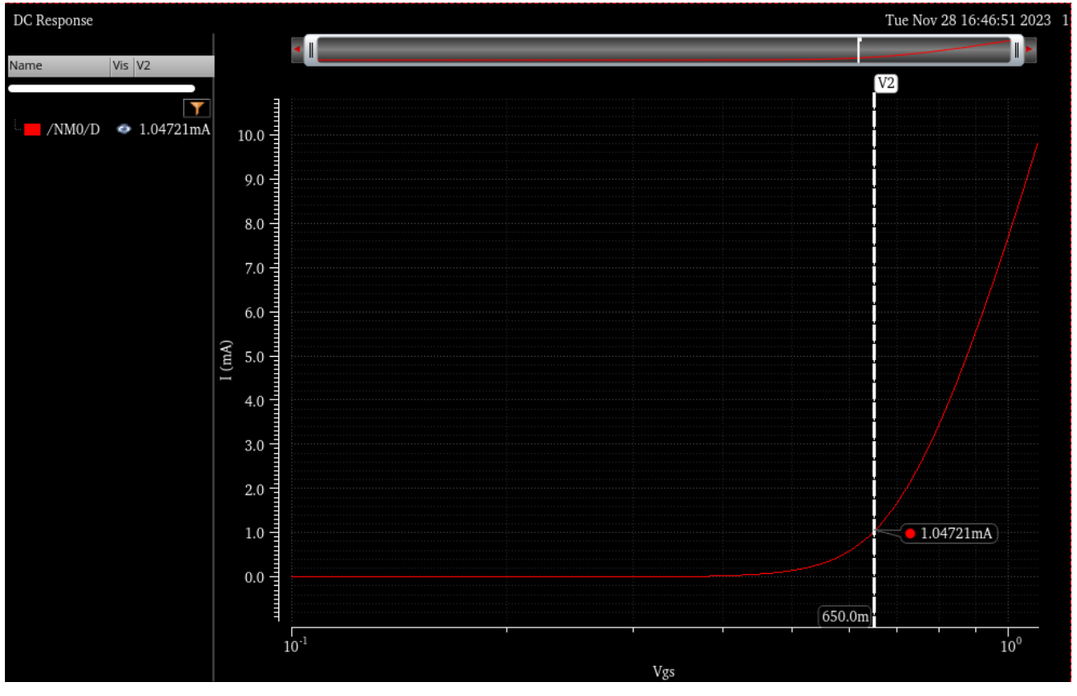
2.a. NMOS *(continued)*

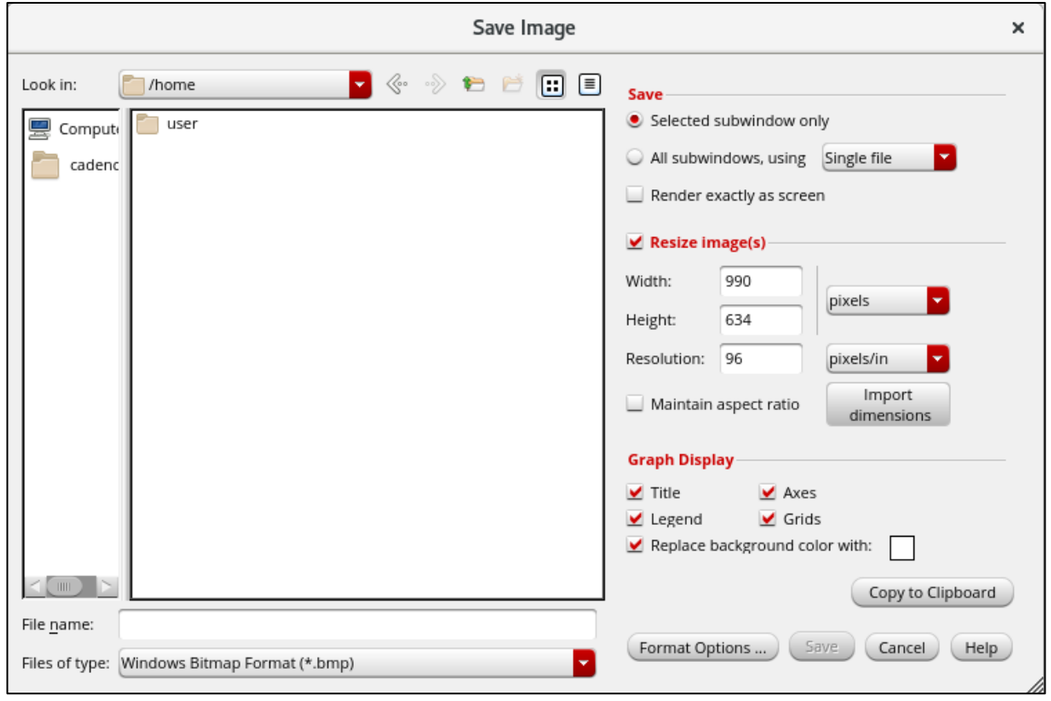
- Now to get ID, set a new **Vertical Marker**, with **X Positions** equal to Vgs (650 mV).
- The value of ID is equal to 1.04 mA.





2.a. NMOS *(continued)*

- To export the waveform, in the VIVA XL Window, select **File → Save Image…**
- Save the image in the desired folder.



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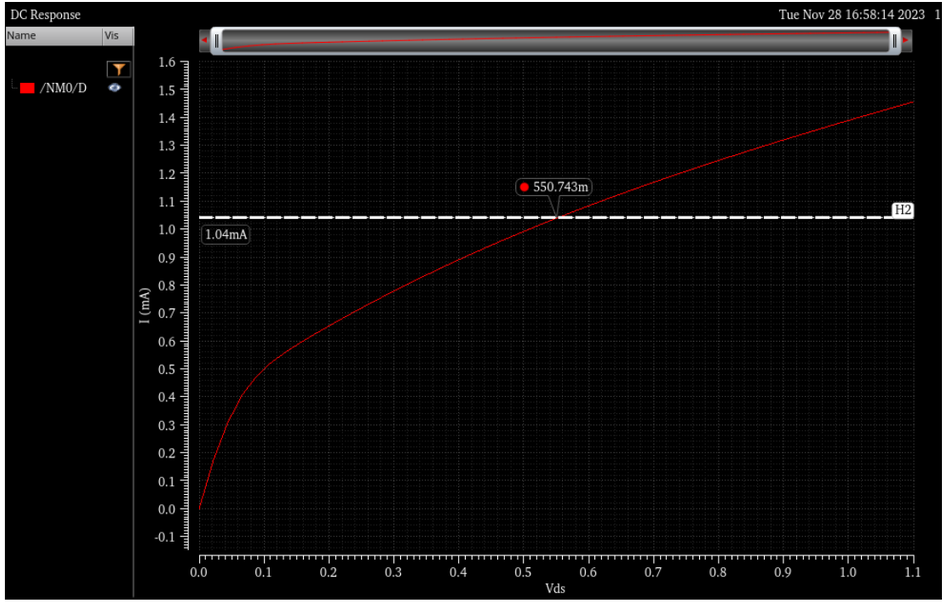
2.a. NMOS *(continued)*

- To find Vds at that current (1.04 mA), we need to sweep Vds.
- Double click on the dc analysis set previously and change the **Variable Name** to **Vds**.
- Change the **Start value** to **0** and the **Sweep Type** to **Automatic**.
- Knowing the value of ID, we set a horizontal marker and find the value of Vds on the plot which is 550.7 mV.



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2.a. NMOS *(continued)*

- Now to check if the transistor is in its saturation region, we need to verify the following conditions:
  - Vgs ≥ Vth ⇔ 650 ≥ 591 (mV)
  - Vds ≥ Vgs – Vth ⇔ 550.7 ≥ 650 – 591 (mV)
- The conditions hold and therefore the nmos transistor is in the saturation region.

- Checking the saturation condition is important before continuing our work because we don't want our transistor to be in the triode region.

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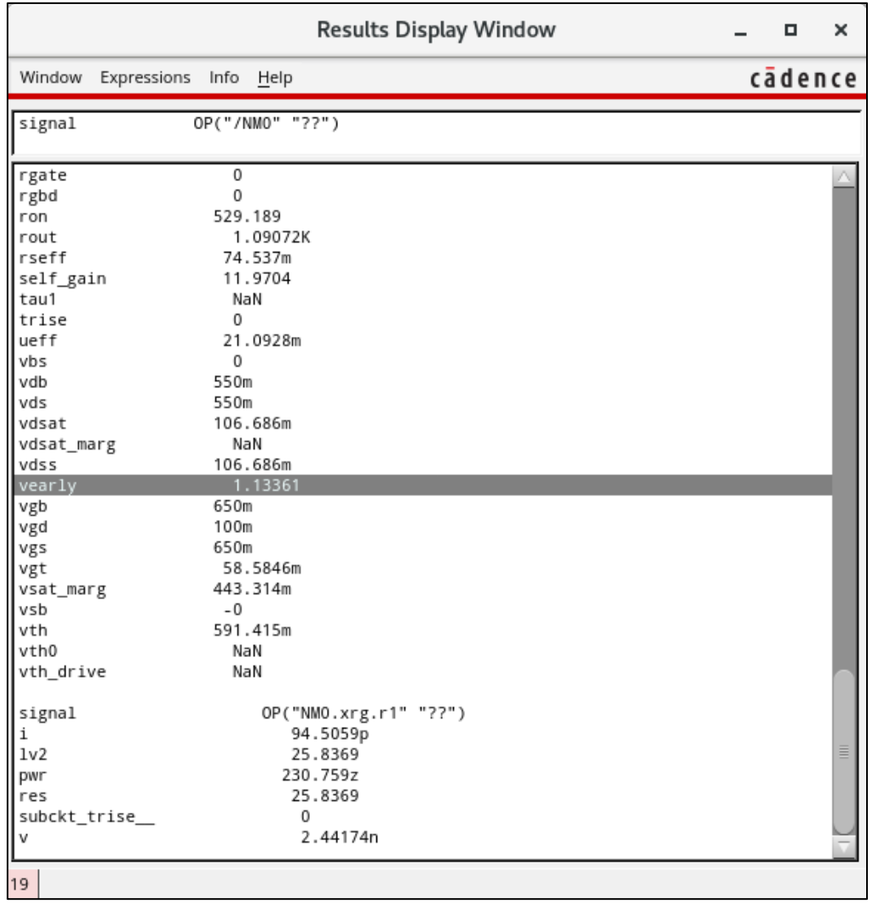
2.a. NMOS *(continued)*

- To find the Early Voltage Va of the nmos transistor we can use either of the two methods described below.

- Method one:
  - In the maestro tab, click on Results → Print → DC Operating Points.
  - Click once on the nmos transistor.
  - The Results Display Window lists all the parameters, including the early voltage which is equal to 1.134 V.



- Run the simulation again, in case you had closed the maestro tab.

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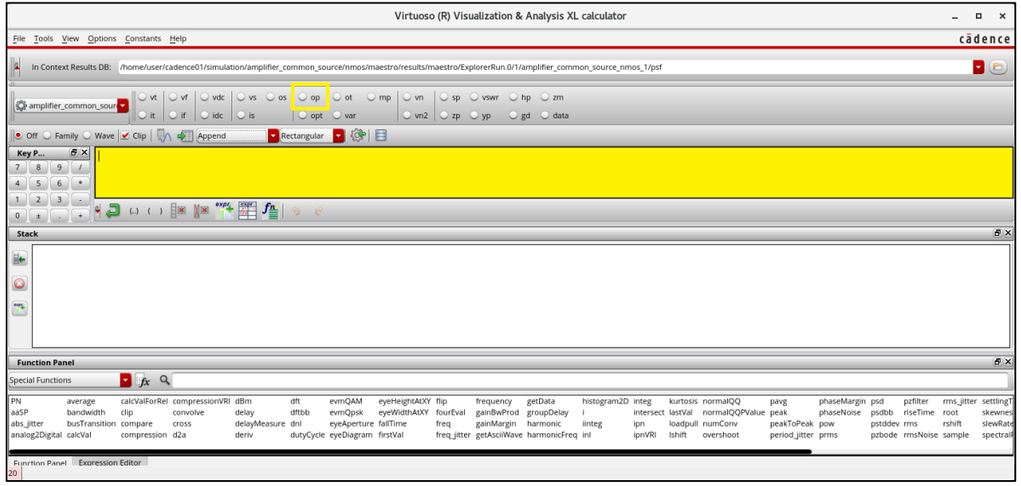
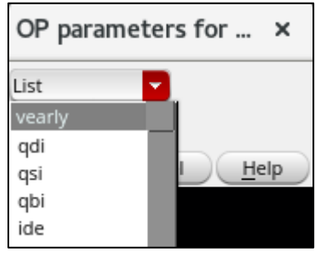
2.a. NMOS *(continued)*

- Method two:
  - We have to use the tool Calculator.
  - From the maestro tab, click on Tools → Calculator.
  - The highlighted field is where we will write the required expression to find the early voltage of the nmos transistor.
  - Click once on “op”, which enables us to select a schematic instance to create an expression for DC operating point.
  - Select the nmos transistor by clicking once on it.
  - Choose “vearly” from the List in the window “OP parameters for NM0” and click OK.
  - The highlighted field of the tool Calculator should have the expression shown in the next slide.





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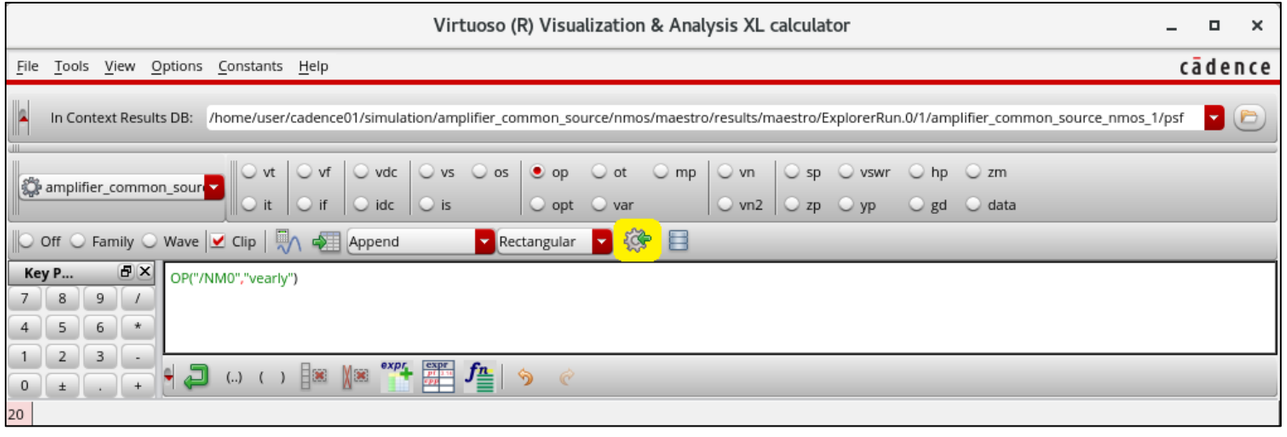
2.a. NMOS *(continued)*

- Click on the highlighted button to send the expression to ADE Outputs.



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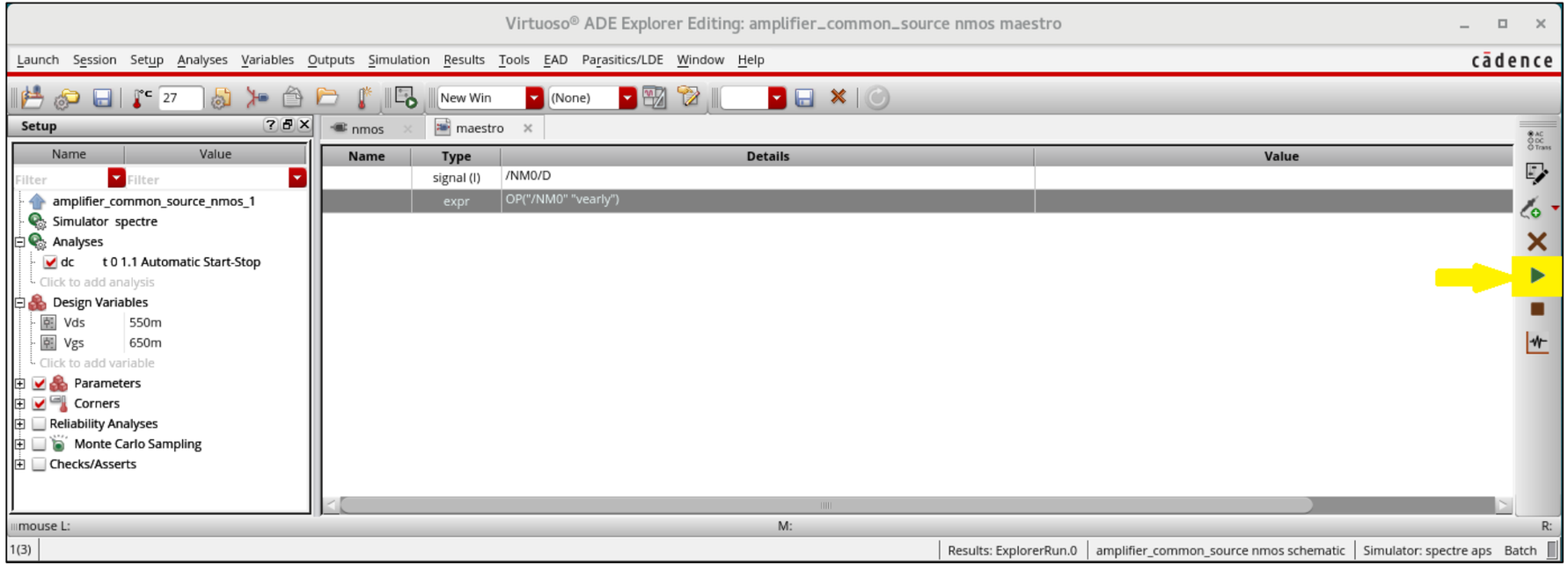
2.a. NMOS *(continued)*

- Run the simulation by clicking on the Netlist and Run button.



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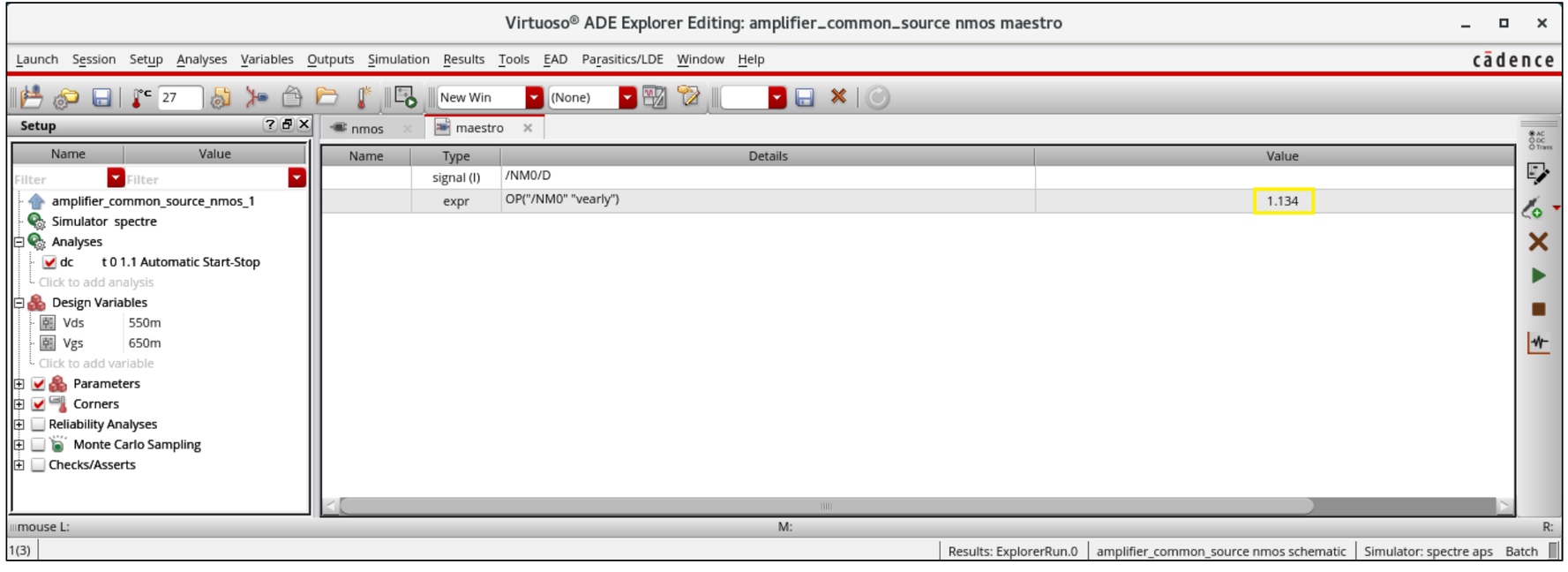
2.a. NMOS *(continued)*

- The value of the early voltage Va is 1.134 V.



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2.a. NMOS *(continued)*

- Now using the previous results, we can get the transistor parameters.
- $\lambda = \frac{1}{|VA|} = \frac{1}{1.134} = 0.881\ V^{-1}$
- $I_D = \frac{1}{2} K'n \frac{W}{L} (Vov)^2 (1 + \lambda\ Vds)\ A$
- $Vov = Vgs - Vth = 650 - 591 = 59\ mV$
- $k'n = \frac{2(L)Id}{W(Vov^2)(1+\lambda V_{ds})} = \frac{2(45n)(1.04m)}{(21.6u)(59m)^2(1+(0.881)(550m))} = 8.4 \times 10^{-4}\ A/V^2$
- $gm = \frac{2(Id)}{Vov} = \frac{2(1.04m)}{59m} = 35.25\ mA/V$

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2.a. NMOS Parameter Summary

Parameter	Value
Wn	21.6 um
Ln	45 nm
Id	1.04 mA
Vov	59 mV
Vth	591 mV
Vgs	650 mV
Vds	550 mV
gm	35.25 mA/V
k’n	0.84 mA/V^2
Va	1.134 V
λ	0.881 1/V

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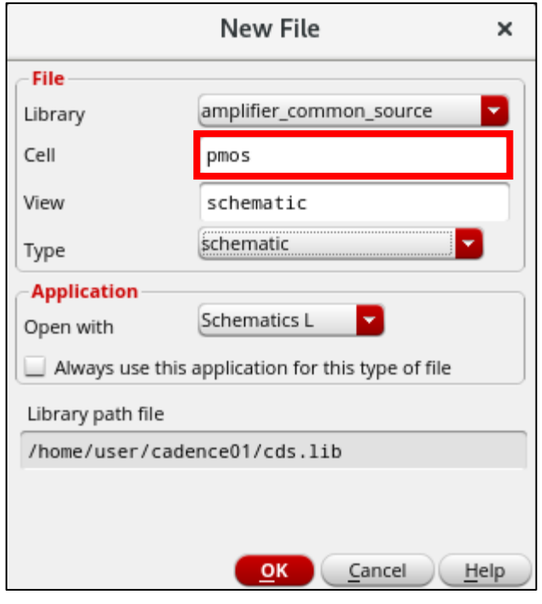
2.b. PMOS

- We will now find the characteristics of the PMOS transistor.
- From the Library Manager, select your library.
- Select **File → New → Cell View**…
- Name the Cell "**pmos**" and click **OK** (make sure both fields Library and Type are as shown below).
- We will go through the same steps as of the NMOS transistor, in order to get the characteristics of the PMOS transistor.



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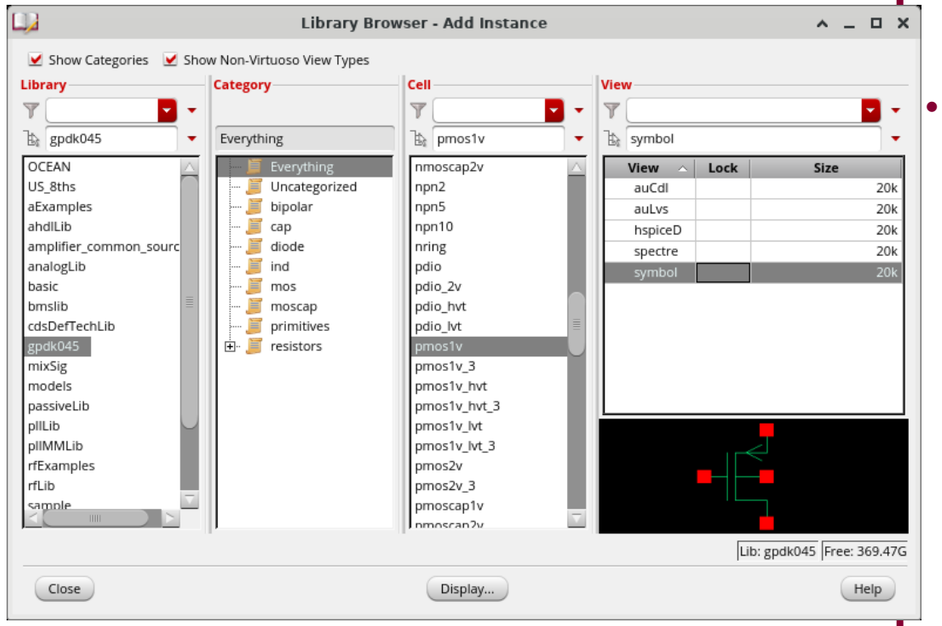
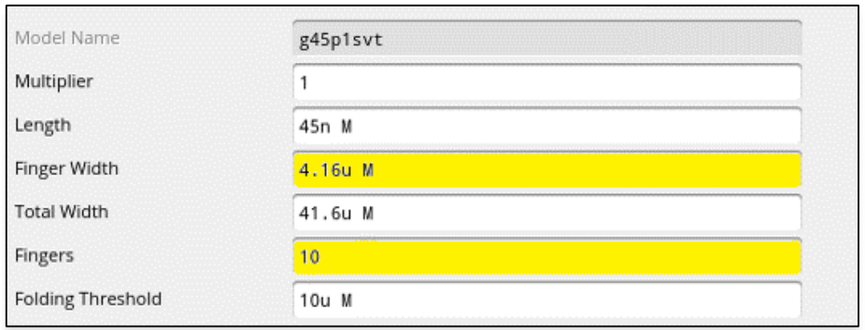
2.b. PMOS *(continued)*

- The PMOS and the NMOS will have the same Vgs, Vds, L and ID.
- **Note that for the PMOS, all the reported voltages are in absolute value.**
- We should repeat the simulations and keep changing the value of the transistor width W until we get the same value of the drain current we got in the NMOS simulation, which was 1.04 mA. The value of W corresponding to a 1.04 mA drain current happened to be 41.6 um.
- So let us start first by setting up the PMOS. Go to **Create → Instance** and browse to get the **pmos1v** transistor.
- After placing the PMOS in the Schematic Editor, select the transistor, then right-click and select **properties**. Set the **Fingers** to **10** and the **Finger Width** to **4.16 um** and click on the enter key on your keyboard.





- The size of the PMOS transistor should be greater than the size of the NMOS transistor if they are to carry the same current with the same terminal voltages since K'p < K'n.

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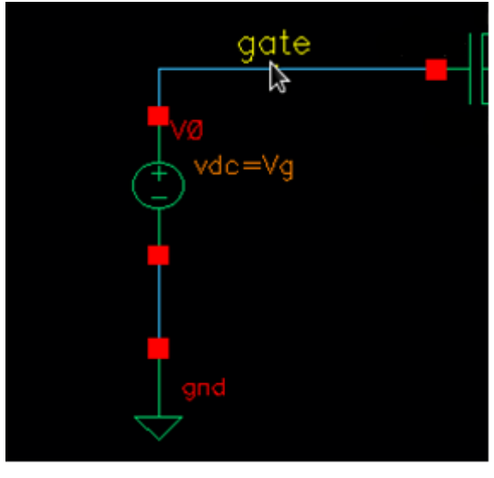
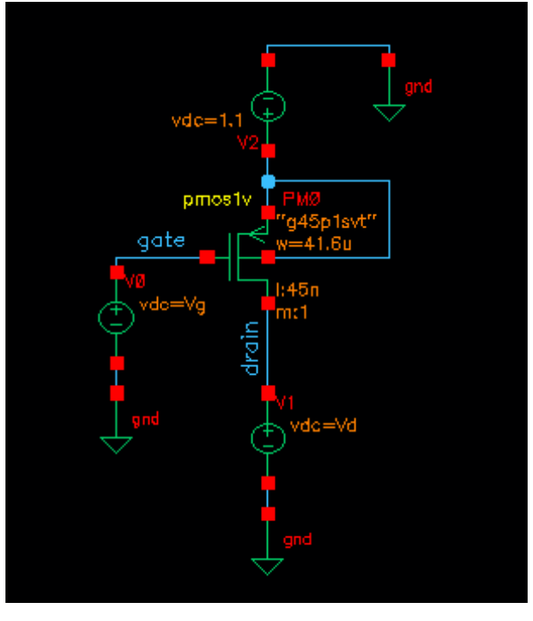
2.b. PMOS *(continued)*

- Place the components as seen in figure below.
- Set the DC voltage values of the gate and drain to Vg and Vd respectively.
- Connect the circuit correspondingly.
- To name the connections ‘gate’ and ‘drain’, click on **Create → Wire Name…**
- Then attach the labels to the respective connections as shown below.





- Don’t forget to flip the voltage source at the source terminal of the transistor.
- Always Check and Save after modifying your circuit.

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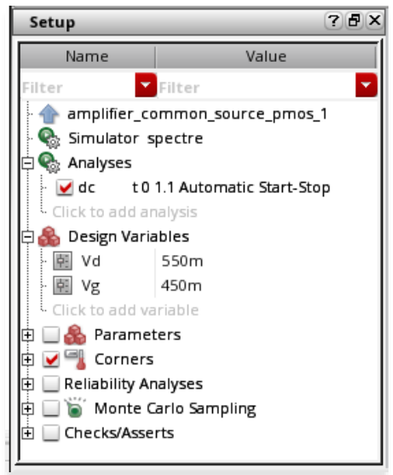
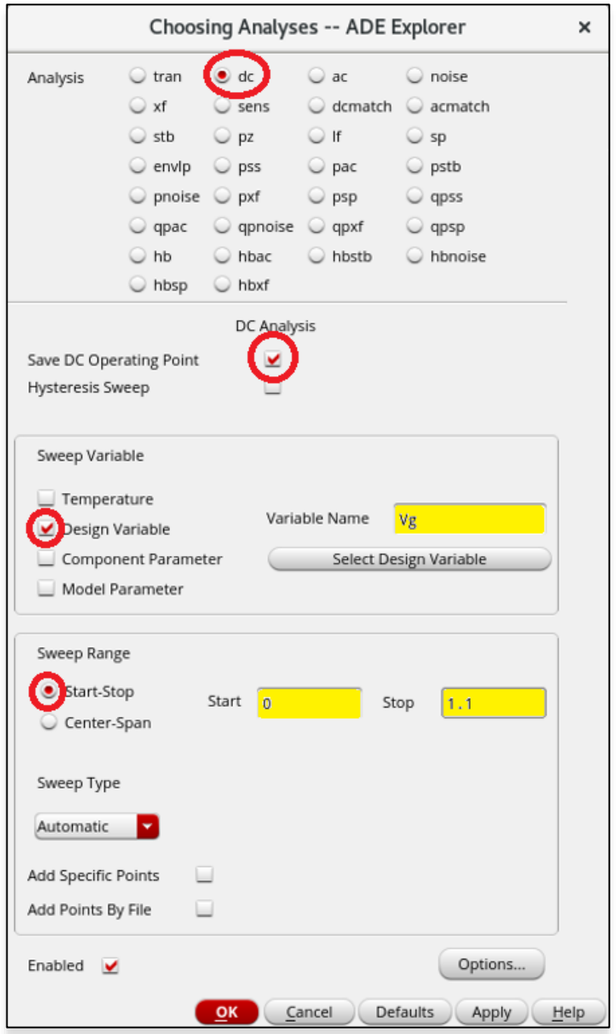
2.b. PMOS *(continued)*

- Launch **ADE Explorer** (Launch → ADE Explorer).
- Select Create New View and click OK.
- Click OK when the “Create new ADE Explorer view” window opens.
- Select **click to add variable → Copy From**
- Set **Vd** to **550 mV** and **Vg** to **450 mV.**
- Select **Analysis → Choose → dc**.
- Check the Save DC Operation Point and set the design variable to **Vg**.
- The **start** and **stop** are set to **0** and **1.1** respectively.





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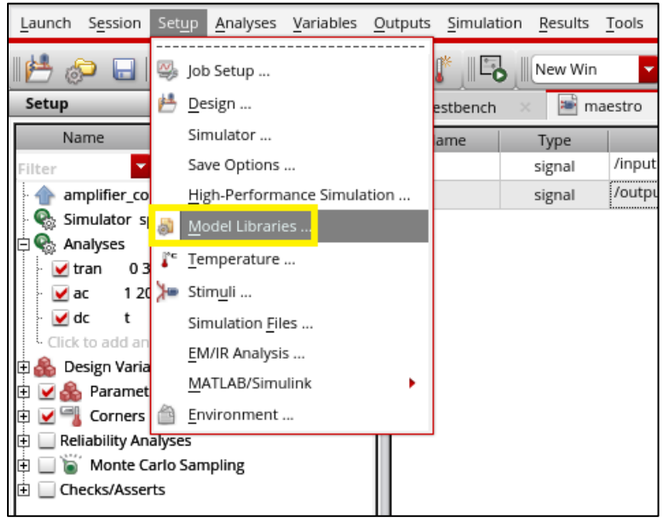
2.a. PMOS *(continued)*

- You still need to add the model files.
- Select **Setup → Model Libraries…**



- Make sure to always change the model library as tt when you open any maestro view.
- The maestro view sets by default the model libraries to mc which is not what we want.

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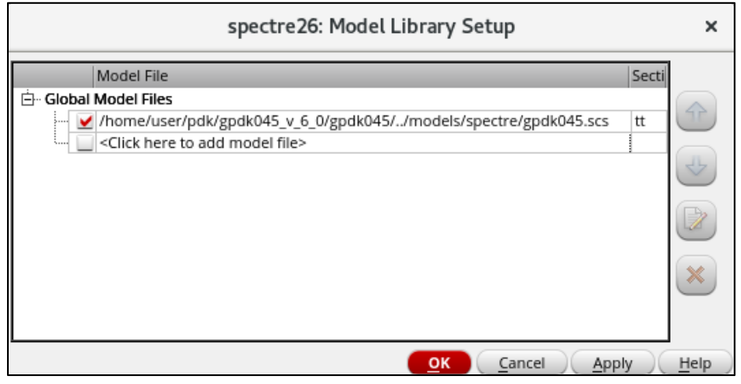
2.a. PMOS *(continued)*

- The tool may have already defined the Model Library.
- If this is the case, the file “gpdk045.scs” will be selected as shown below.
- Click on the **Section** field and **select** “tt” from the drop-down list.
- Click **OK** to save your “Model Library Setup”.



- If the tool hasn’t defined the Model Library, the next few slides explain how to select the file “gpdk045.scs”.

- Make sure to always change the model library as tt when you open any maestro view.
- The maestro view sets by default the model libraries to mc which is not what is needed for real world applications.

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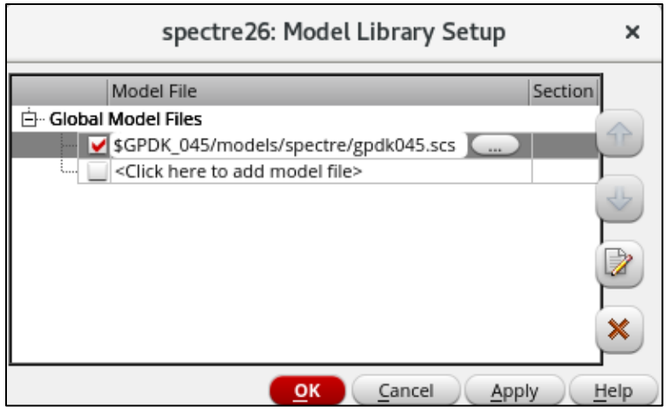
2.a. PMOS *(continued)*

- When the “Model Library Setup” form pops-up, click on <Click here to add model file>.
- **Enter** the following directory:

“*$GPDK_045/models/spectre/gpdk045.scs*”

- *Note that the “GPDK_045” must point to the root folder of the pdk, “gpdk045_v_6_0”.*



- Make sure to always change the model library as tt when you open any maestro view.
- The maestro view sets by default the model libraries to mc which is not what is needed for real world applications.

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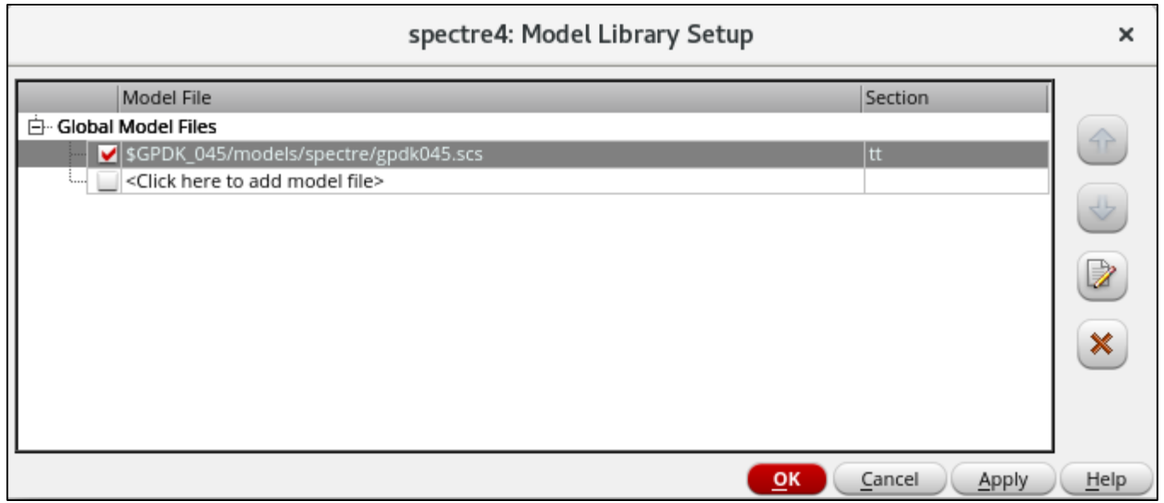
2.a. PMOS *(continued)*

- Click on the **Section** field and **select** “tt” from the drop-down list.
- Click **OK** to save your “Model Library Setup”.



- Make sure to always change the model library as tt when you open any maestro view.
- The maestro view sets by default the model libraries to mc which is not what is needed for real world applications.

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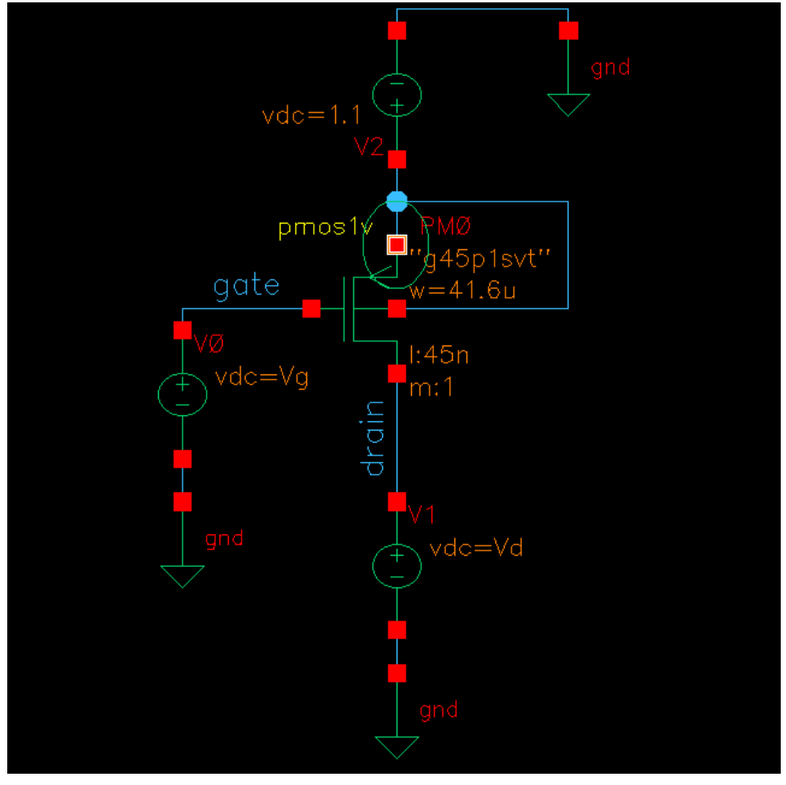
2.b. PMOS *(continued)*

- To plot the voltage Vgs vs. current, select **Output → To Be Plotted → Select on Design** and click once the red terminal of the source current.
- Note that the drain and source current are the same.
- Vgs is the absolute value of (1.1-Vg). To plot the Vgs vs. the source current, we have to use the tool **Calculator**. This is explained in the next few slides.



- Remember that choosing the red terminal as output means current and choosing the connection means voltage.

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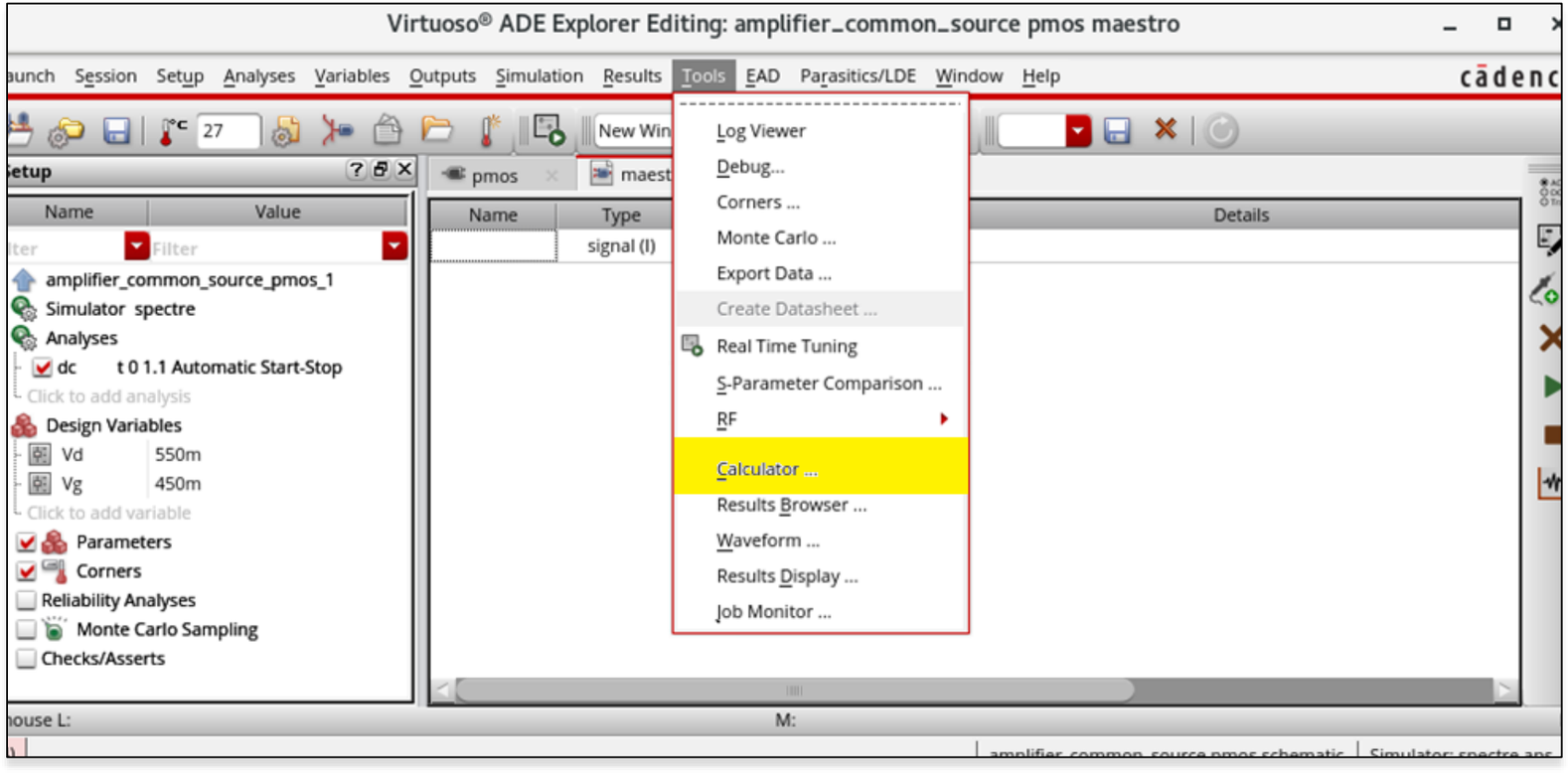
2.b. PMOS *(continued)*

- From **ADE Explorer,** click on **Tools → Calculator.**



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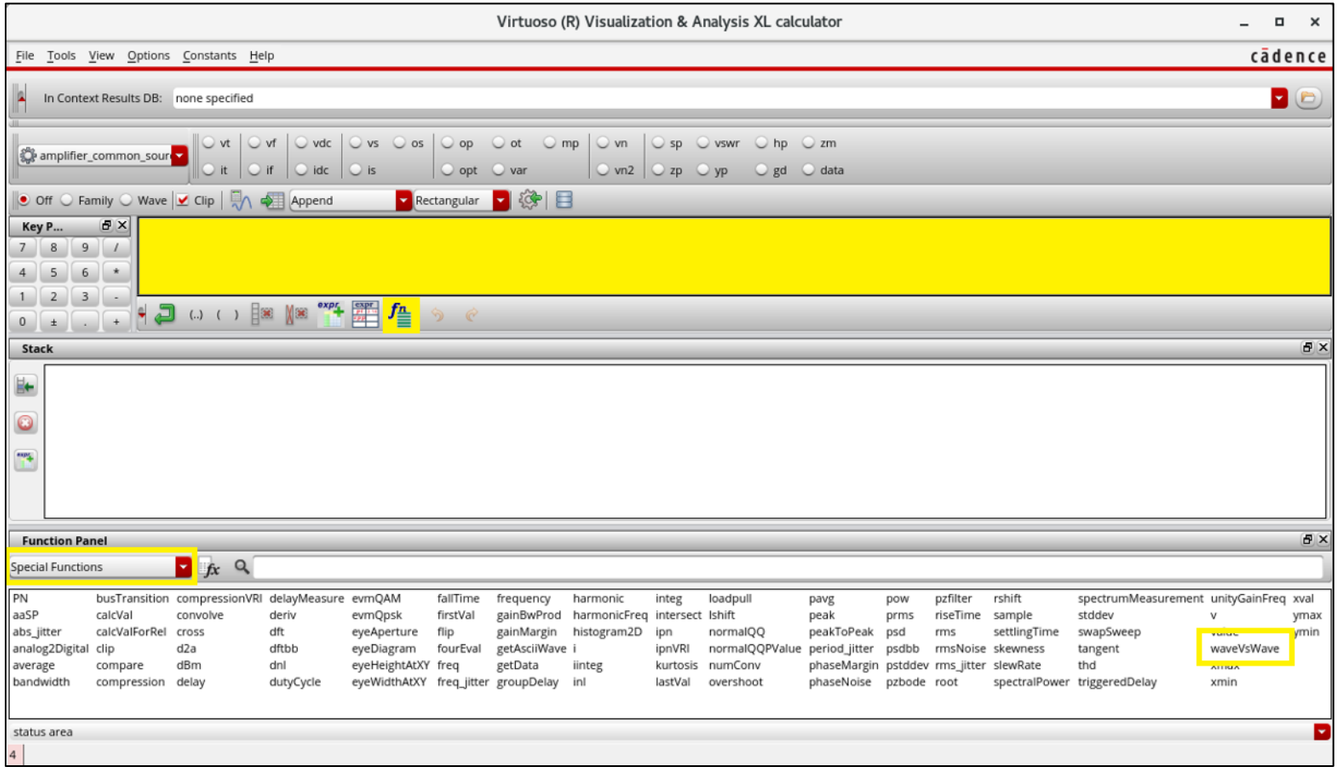
2.b. PMOS *(continued)*

- The highlighted field in yellow is where we can write the functions or equations.
- From the drop-down list in the **Function Panel**, select **Special Functions**, then click on **waveVsWave**, as shown below.



- If the Function Panel is not shown, click on the highlighted button "**f_n**".

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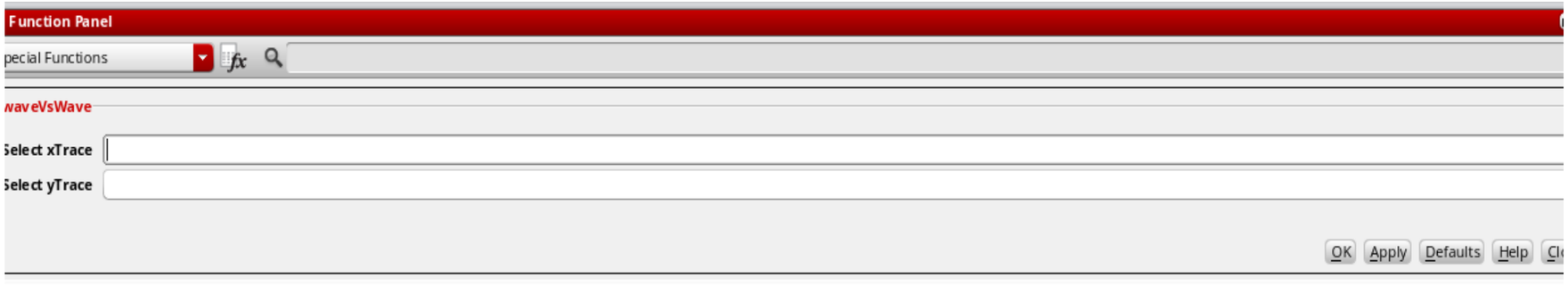
2.b. PMOS *(continued)*

- The **waveVsWave** window appears.
- We have to create expressions for the **xTrace** and the **yTrace.**
- We have to use the highlighted part that was shown in slide 42, in order to fill in both traces.



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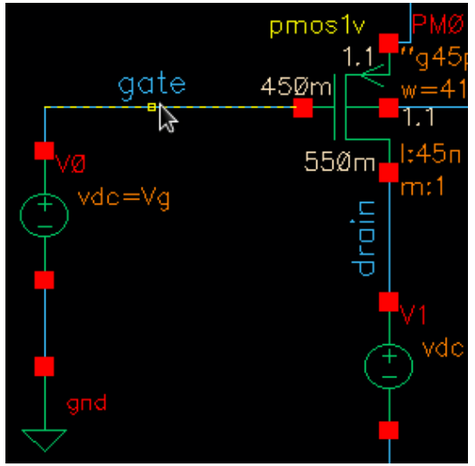
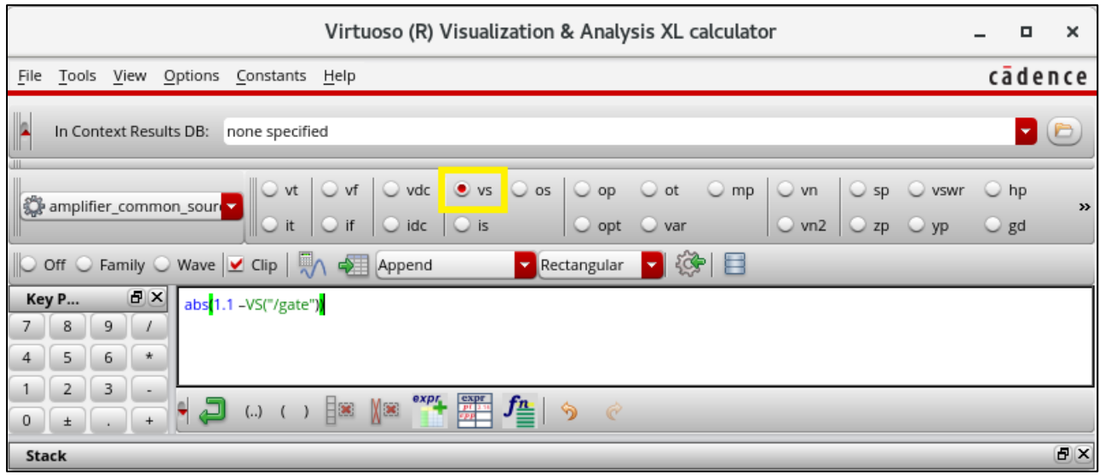
2.b. PMOS *(continued)*

- First, type '**`abs(1.1 –`** ' in the highlighted box, then click on **vs** (shown in figure).
- Clicking on **vs** will allow us to select a schematic **signal** to create an expression for DC sweep **voltage**.
- Select the connection named '**gate**', add a ') ' to close the **abs** expression.
- Now the expression should be as below.
- This expression is the **xTrace.** Cut the expression and paste it in the **xTrace** box.





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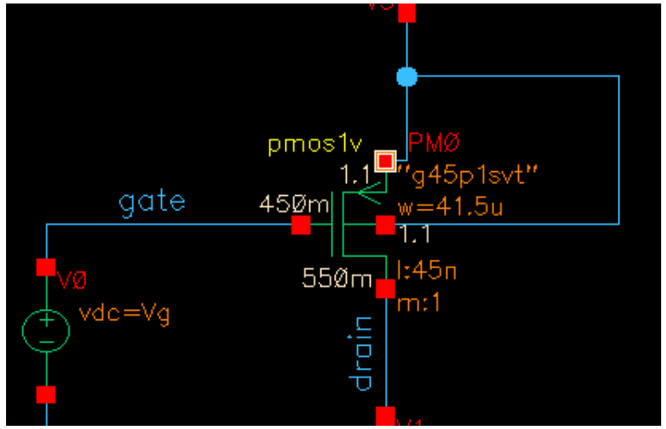
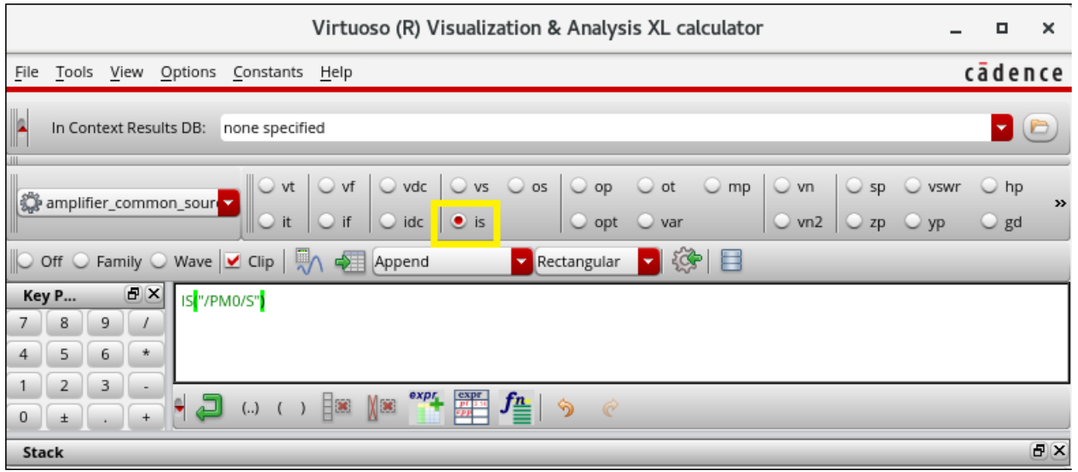
2.b. PMOS *(continued)*

- Now for the **yTrace**, click on **is** (shown in figure).
- Clicking on **is** will allow us to select a schematic **terminal** to create an expression for DC sweep **current**.
- Select the **red terminal** of the source.
- The expression should be as below.
- This expression is the **yTrace.** Cut the expression and paste it in the **yTrace** box.





cadence

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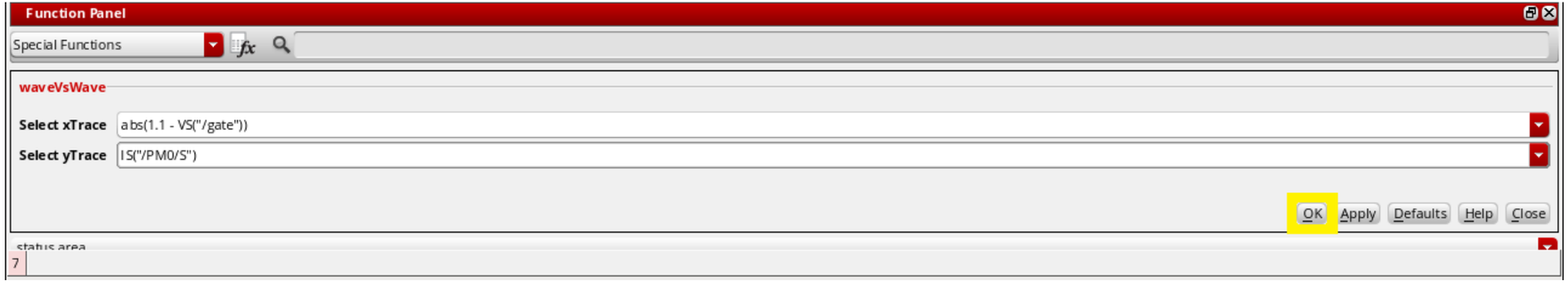
- NMOS
- PMOS
- CS Amplifier
- Symbol
- Test Bench

2.b. PMOS *(continued)*

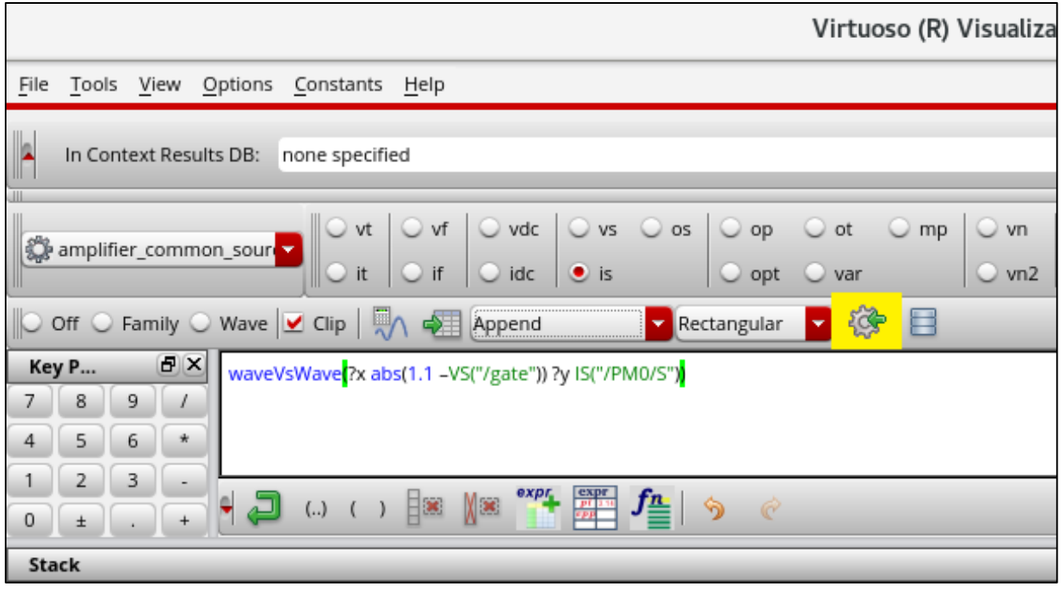
- Now the **waveVsWave** window should be as below.
- Click **OK**.



cadence

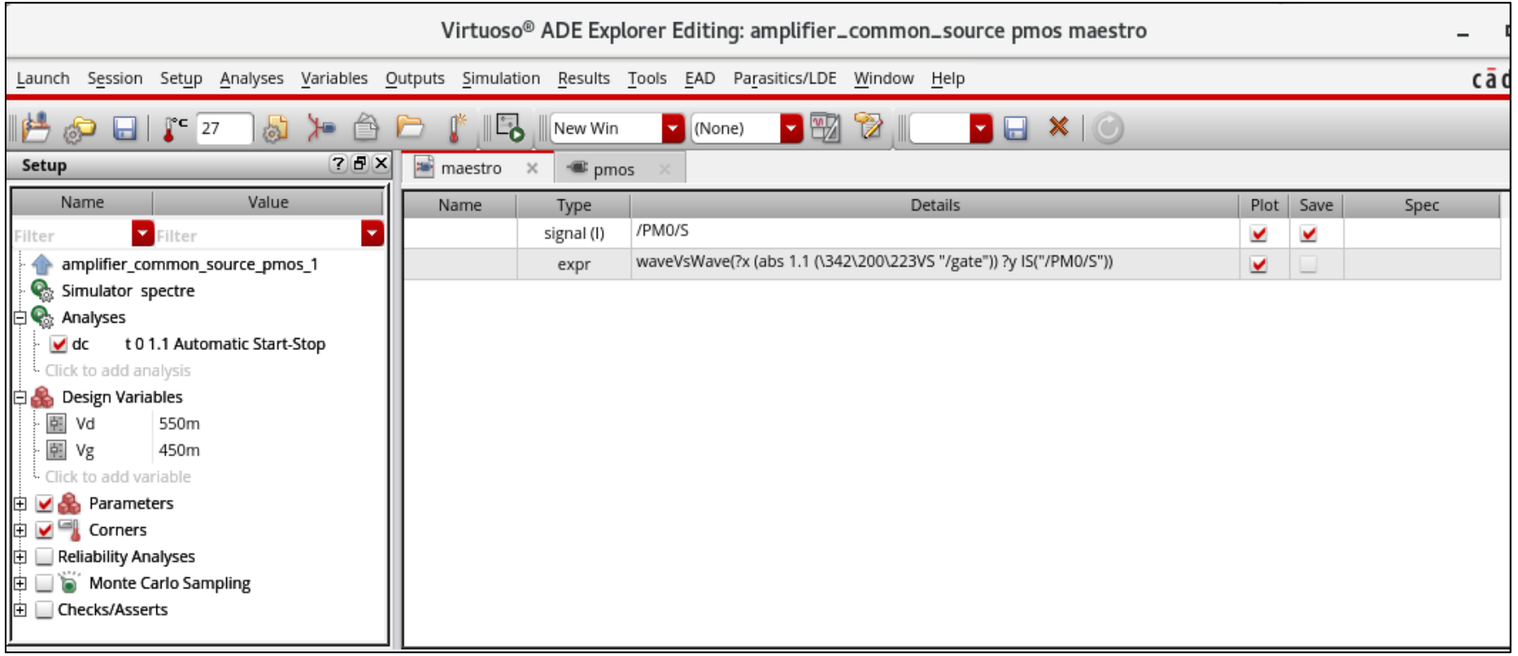
2.b. PMOS *(continued)*

- After clicking OK**,** the whole expression should appear in the highlighted field mentioned earlier.
- In order to send the expression to **ADE Explorer**, click on the highlighted button.



2.b. PMOS *(continued)*

- **ADE Explorer** should be as below.
- Click on the **Netlist and Run** button to run the simulation.



- The process condition (section) used for the simulations should be “tt” not “mc”. Check slide 23 to see how to change it from Setup → Model Libraries.

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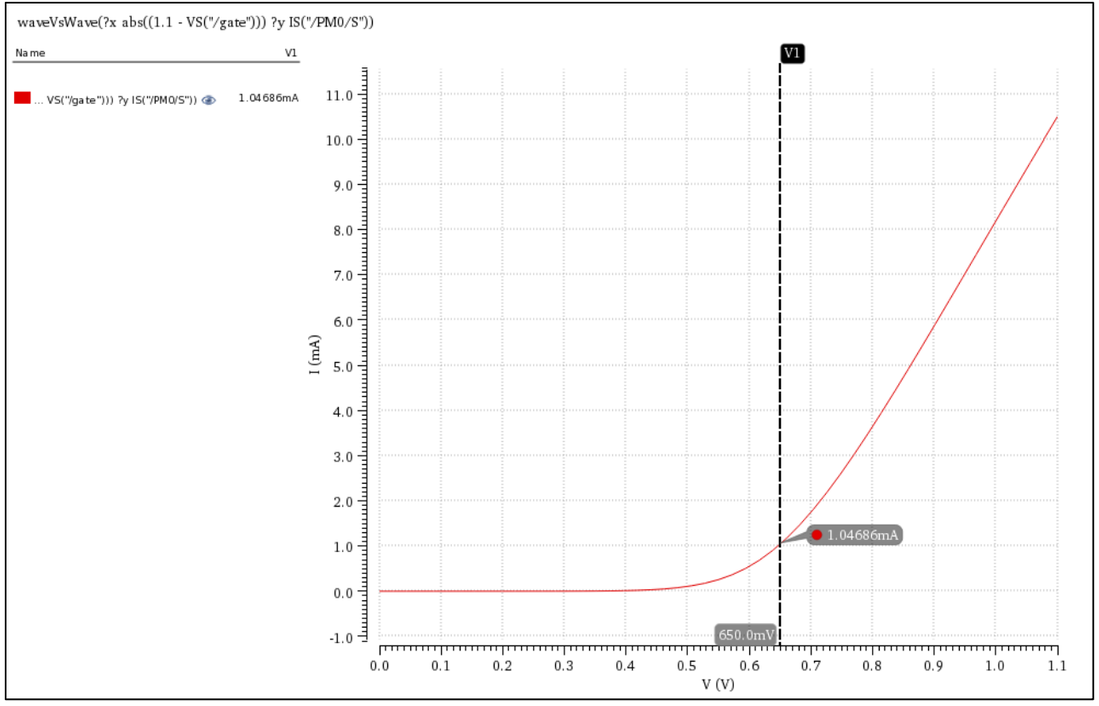
2.b. PMOS *(continued)*

- To see the value of Id we got, we should set a marker at Vgs which is 650mV as we did in the NMOS simulation.
- **Marker → Create Marker → Vertical** and set the **X Positions** to 650 mV.
- We can see from the plot that the value of the current is approximately 1.04 mA.



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2.b. PMOS *(continued)*

- Note that we need to get a value of Id which is approximately equal to the value of the current gotten from the NMOS simulation.

- If the value of the current we got happened to be greater than the value we are expecting, we should reduce the width of our transistor because the current is directly proportional to the transistor's size according to the following equation.

$$I_D = \frac{1}{2} K'p \frac{W}{L} (|Vov|)^2 (1 + \lambda |Vds|) \quad A$$

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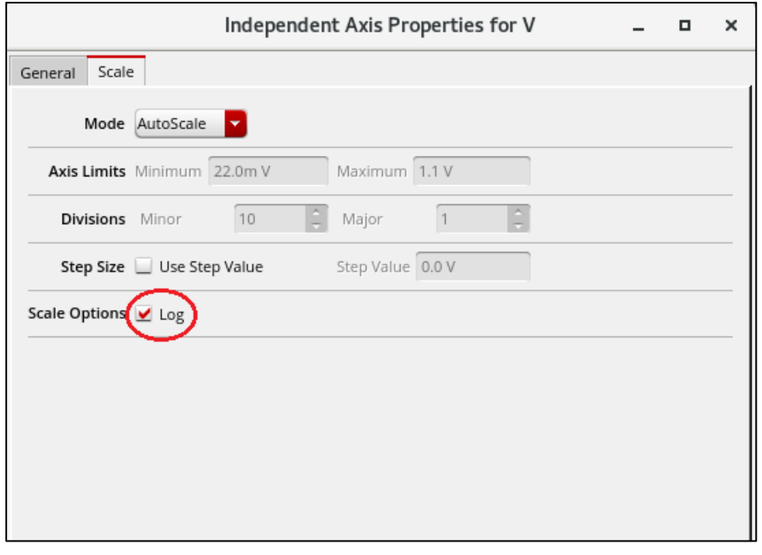
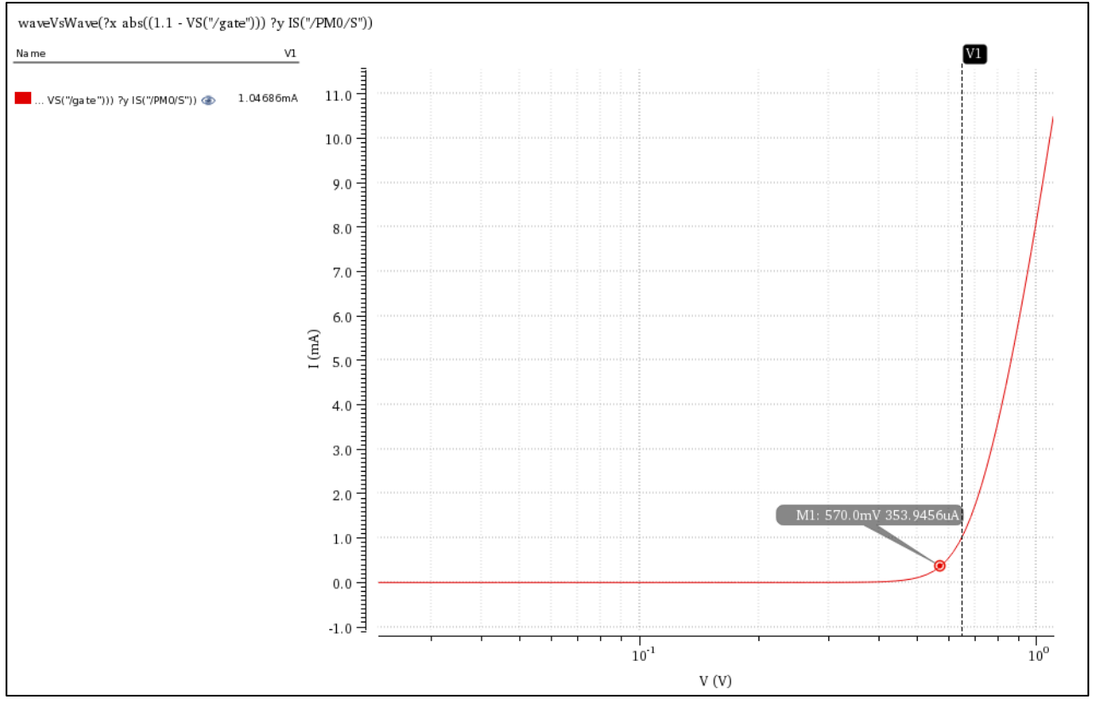
2.b. PMOS *(continued)*

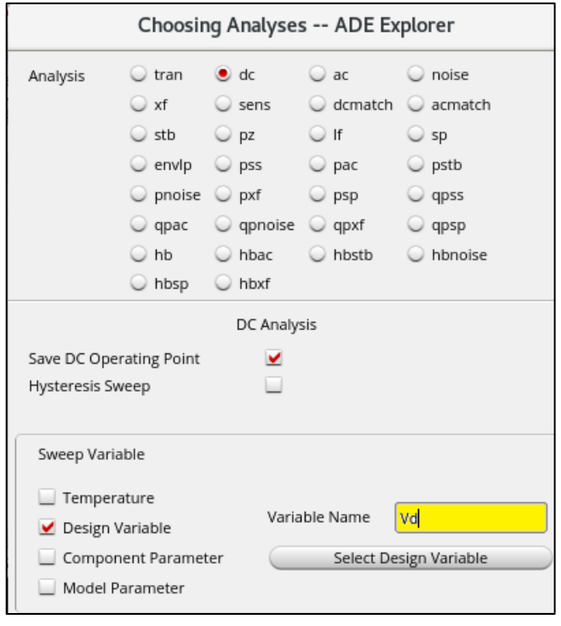
- On the same plot, double click on the x-axis and set the scale to logarithmic.
- Create a marker and place it at the point where the curve starts going up. This is the value of the threshold voltage Vth which is 570 mV.

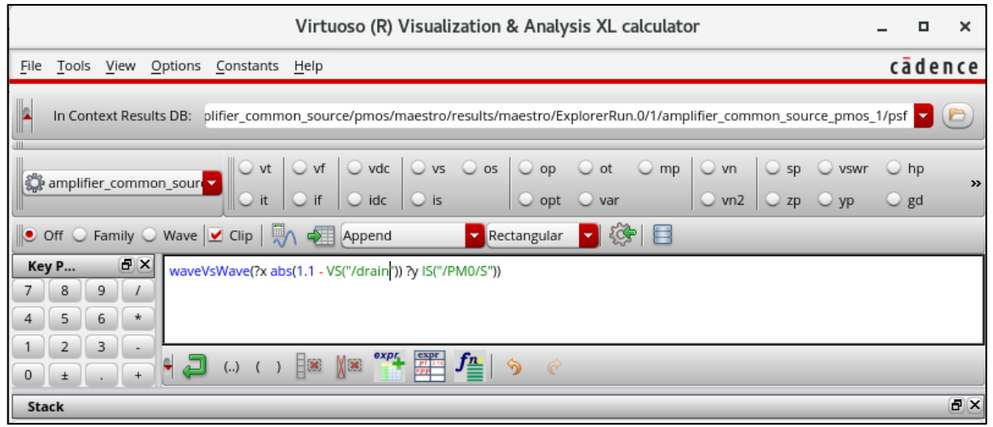


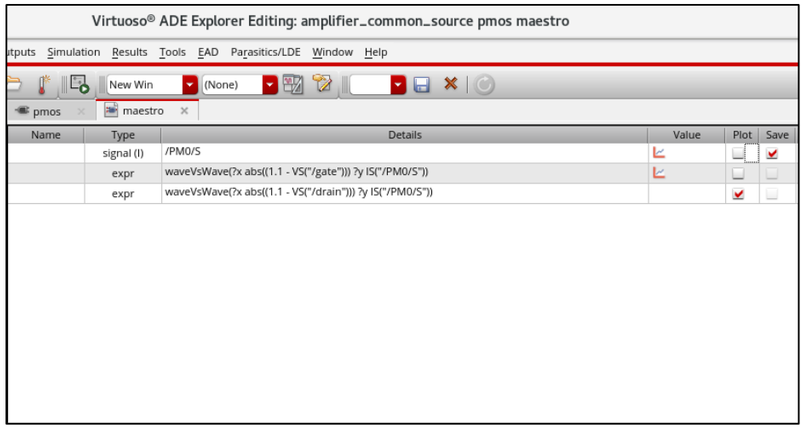


2.b. PMOS *(continued)*

- Now to get Vds, we have to change the **Variable Name** in slide 39 to **Vd**.
- Repeat the same steps of the waveVswave function and select the “drain” connection instead of the “gate” connection.
- Then the final expression in slide 47 has to be:
  `waveVsWave(?x abs(1.1 - VS("/drain")) ?y IS("/PM0/S"))`
- **ADE Explorer** should be as below. Click on the **Netlist and Run** button to run the simulation.







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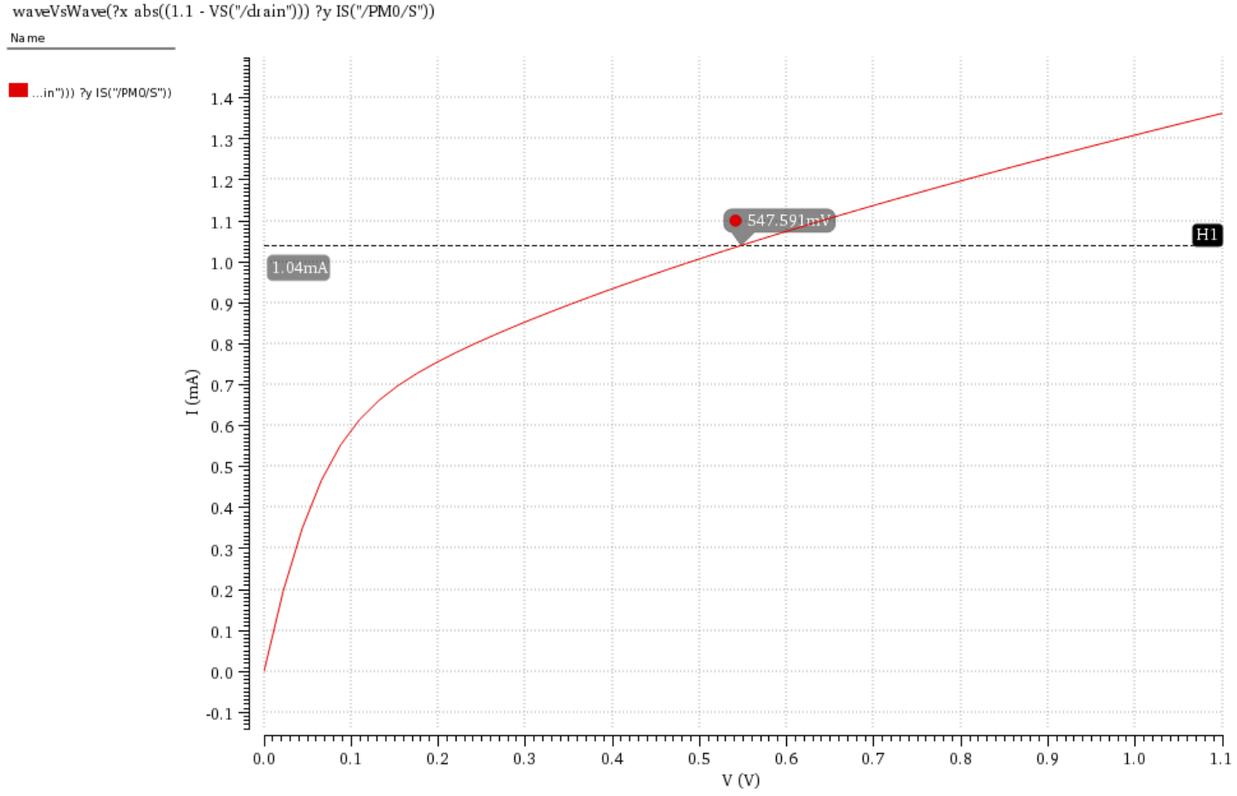
2.b. PMOS *(continued)*

- Knowing the value of Id, we set a horizontal marker and find the value of Vds on the plot which is 548 mV.



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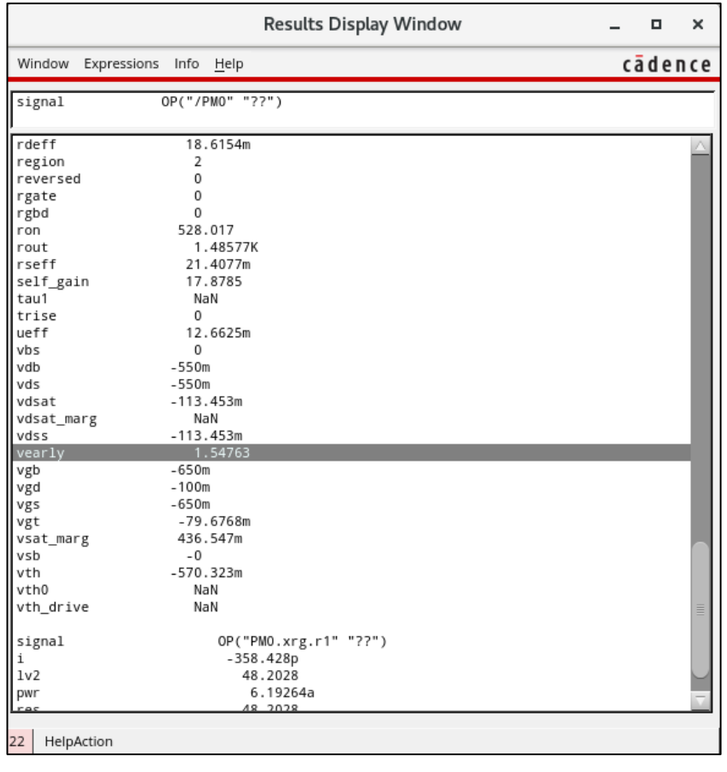
2.b. PMOS *(continued)*

- To find the value of the early voltage of the pmos transistor, we can use either of the two methods explained earlier in the nmos section.
- Using the first method, from the maestro tab, Results → Print → DC Operating Points and click on the pmos, we find the early voltage Va of the pmos to be 1.55 V.



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2.b. PMOS *(continued)*

- Check the saturation conditions:
  - Vsg ≥ |Vth| ⇔ 650 ≥ 570 (mV)

    or Vgs ≤ Vth ⇔ – 650 ≤ – 570 (mV)
  - Vsd ≥ Vsg – |Vth| ⇔ 548 ≥ 650 – 570 ≥ 80 (mV)

    or Vds ≤ Vgs – Vth ⇔ – 548 ≤ – 650 + 570 ≤ – 80 (mV)

  The saturation conditions are true.
- Now for the DC parameters of the transistor:

$$|Vov| = Vsg - |Vth| = 650 - 570 = 80\,mV$$

$$\mathrm{gm} = \frac{2Id}{Vov} = \frac{2(1.04m)}{80m} = 26\,mA/V$$

$$\lambda = \frac{1}{|Va|} = \frac{1}{1.55} = 0.645\ 1/V$$

$$\mathrm{k'p} = \frac{2(L)Id}{W(Vov^2)(1+\lambda V_{ds})} = \frac{2(45n)(1.04m)}{(41.6u)(80m)^2(1+(0.645)(548m))} = 2.6 \times 10^{-4}\ A/V^2$$

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2.b. PMOS Parameter Summary *(continued)*

Parameter	Value
Wp	41.6 µm
Lp	45 nm
Id	1.04 mA
Vov	80 mV
Vth	570 mV
Vgs	650 mV
Vds	548 mV
gm	26 mA/V
k’p	0.26 mA/V^2
Va	1.55 V
λ	0.645 1/V

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2.c. Common Source Amplifier

- From the Library Manager, **click** on your library, then File → New → Cell View. Name the new cell view “cs_amplifier”.
- Create the circuit in the next slide. This circuit consists of a current mirror and a common source amplifier.
- We can flip the transistor direction by clicking on “sideways” before placing it in the Schematic Editor. Also, we have to flip the voltage source at the source of the PMOS transistors.
- The resistor **resnsppoly** is found in the gpdk045 library. We will use it instead of a regular resistor to be able to use it in the Layout GXL tool, which will be explained later in the modules.
- The value of the resistor chosen is $\mathbf{430\ \Omega}$.
- To be able to set the resistor value, change the **Calculated Parameter** (in Properties) to **Length** instead of Resistance.
- In order to obtain a current of 1.04 mA at the source of “PM0” of width equal to 41.6 µm, it is important to have 450 mV at the gate of “PM0” (or “PM1”), Thus, we must adjust the width of PM1 to 30.9 µm, to achieve approximately 450 mV at the gate of PM1.

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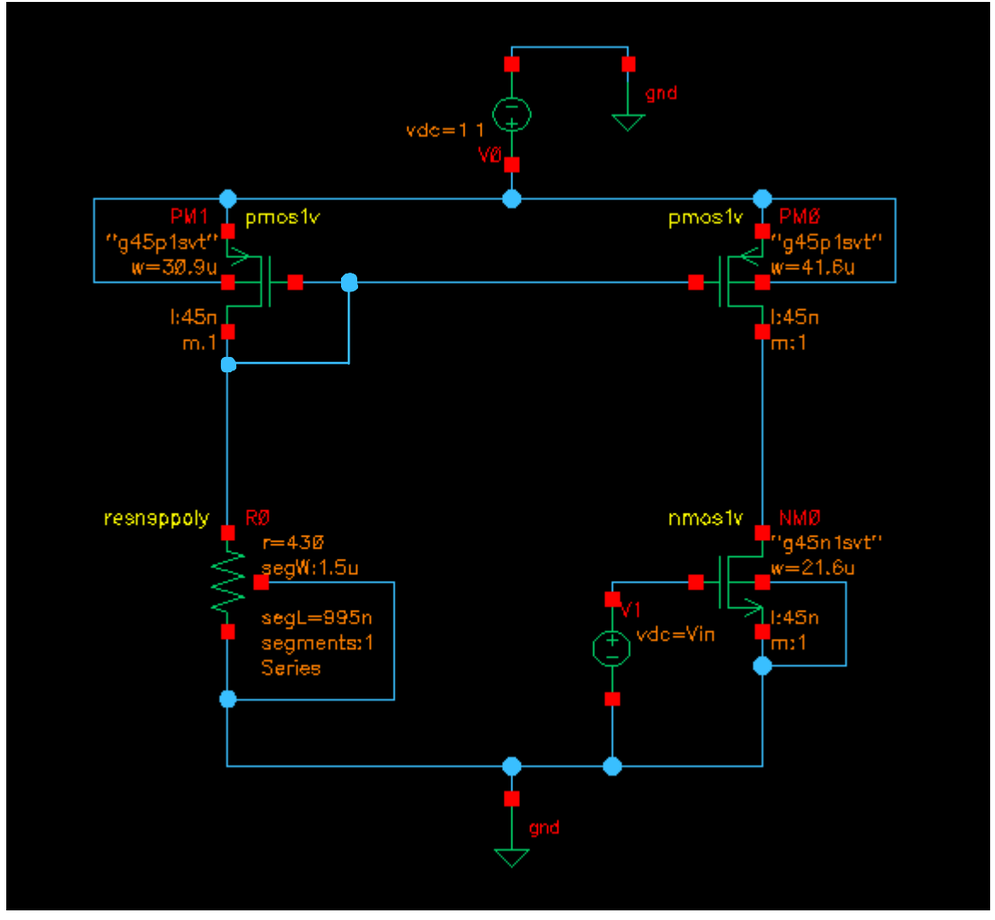
2.c. Common Source Amplifier *(continued)*

- PM0:
  - Fingers = 10
  - Finger Width = 4.16 µm
  - Length = 45 nm
  - Gate connection: Bottom
  - S/D connection: Both
- PM1:
  - Fingers = 10
  - Finger Width = 3.09 µm
  - Length = 45 nm
  - Gate connection: Top
  - S/D connection: Both
- NM0:
  - Fingers = 10
  - Finger Width = 2.16 µm
  - Length = 45 nm
  - Gate connection: Bottom
  - S/D connection: Both



- Set the value of the gate voltage of the NMOS to Vin. This will be our input voltage for the amplifier.
- vdc = 1.1V
- R0 = 430 Ω

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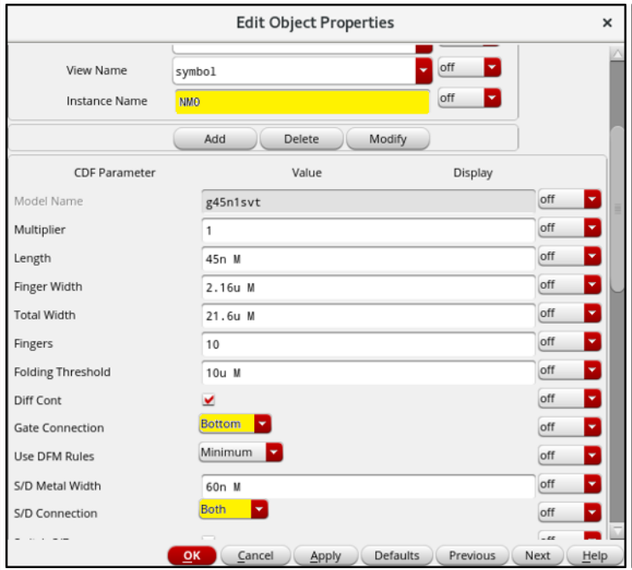
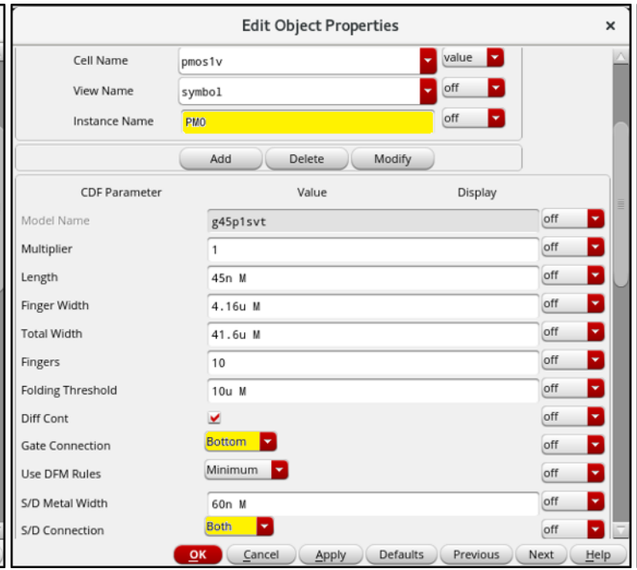
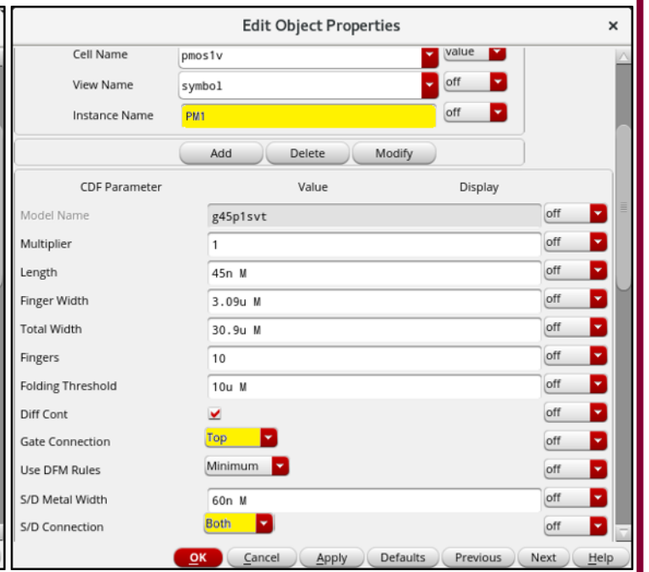
2.c. Common Source Amplifier *(continued)*

- We adjust the Gate Connection and the S/D Connection for the transistors, because when we design the common source amplifier using the Layout GXL tool (Module 7), the terminals will be automatically generated for each transistor.
- Adjust the connections as shown below from the properties form of each transistor.







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2.c. Common Source Amplifier *(continued)*

- Since this is a direct coupled design, before running the DC analysis, we have to model the input resistance of the load by adding a resistor at the output node.
- If the load exhibits itself as a resistor which is not much larger than the output resistance of the amplifier, the aspect ratios of the output transistors should be adjusted in order to keep the same output DC voltage.
- In the following sections, we will place the circuit that we have just built into a symbol and use it as an amplifier. The output of the symbol will have the load resistance; thus, we must take the value of this resistance into account while calculating our parameters.
- The current of the PMOS and NMOS are the same. But after adding the load resistance, the current coming from the PMOS will be split into the resistor and the NMOS.

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2.c. Common Source Amplifier *(continued)*

- A 100 kΩ resistor is used at the load.
- We want our output DC voltage to stay constant at 550mV, which is in the middle of the power source 1.1 V and the ground 0 V.
- Using Ohm's law, the current passing into the load is $I = \frac{V}{R} = \frac{550m}{100k} = 5\ \mu A$.
- The current passing through the NMOS transistor will be obtained using Kirchhoff's Current Law; $I(Nmos) = I(Pmos) - I(load) = 1.04m\ - 5\mu = 1.035\ mA$.
- To accommodate for this change in current we have to change the width of the NMOS transistor because as stated previously the width and the current are directly proportional.
- Using the following equation: $Id = \frac{1}{2} k'n \frac{W_n}{L} Vov^2 (1 + \lambda \text{Vds})$

$$W_n = \frac{2 \times L \times Id}{k'n(Vov)^2(1 + \lambda Vds)} = \frac{2\ (45n)(1.035m)}{(8.4 \times 10^{-4})(59m)^2(1 + (0.881)(550m))} = 21.45\ \mu m$$

- Replacing the value of W of the NMOS transistor and adding the load resistance, we get the circuit shown in the next slide.

- Note that the load resistance is not a part of our inner circuit and will not be modeled in the layout part so here we will model it as an ideal resistor "res" from the analogLib.

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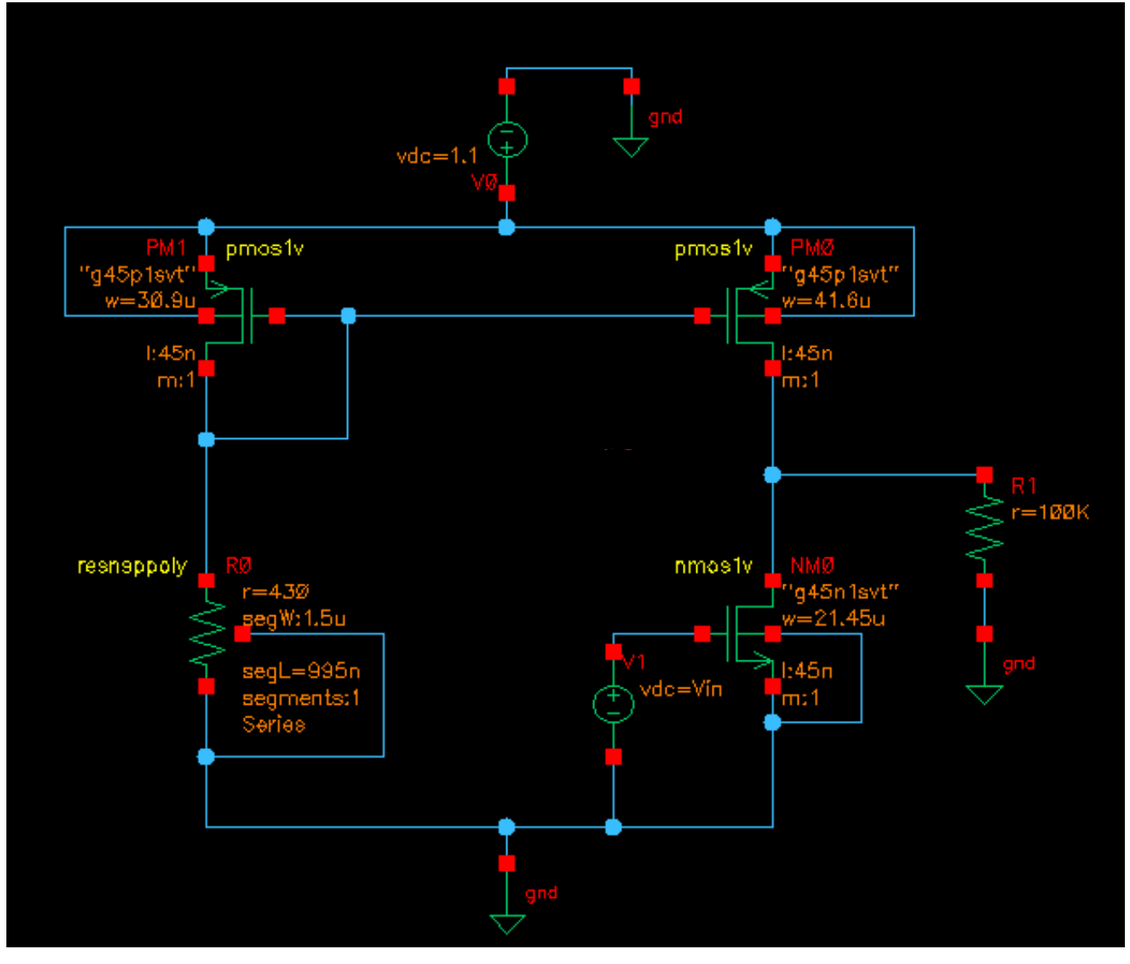
2.c. Common Source Amplifier (continued)

- NM0:
  - Total Width = 21.45 µm
- R1:
  - Resistance = 100 KΩ



- Make sure to connect the gate of PM1 to the Drain terminal to ensure better performance and stability.

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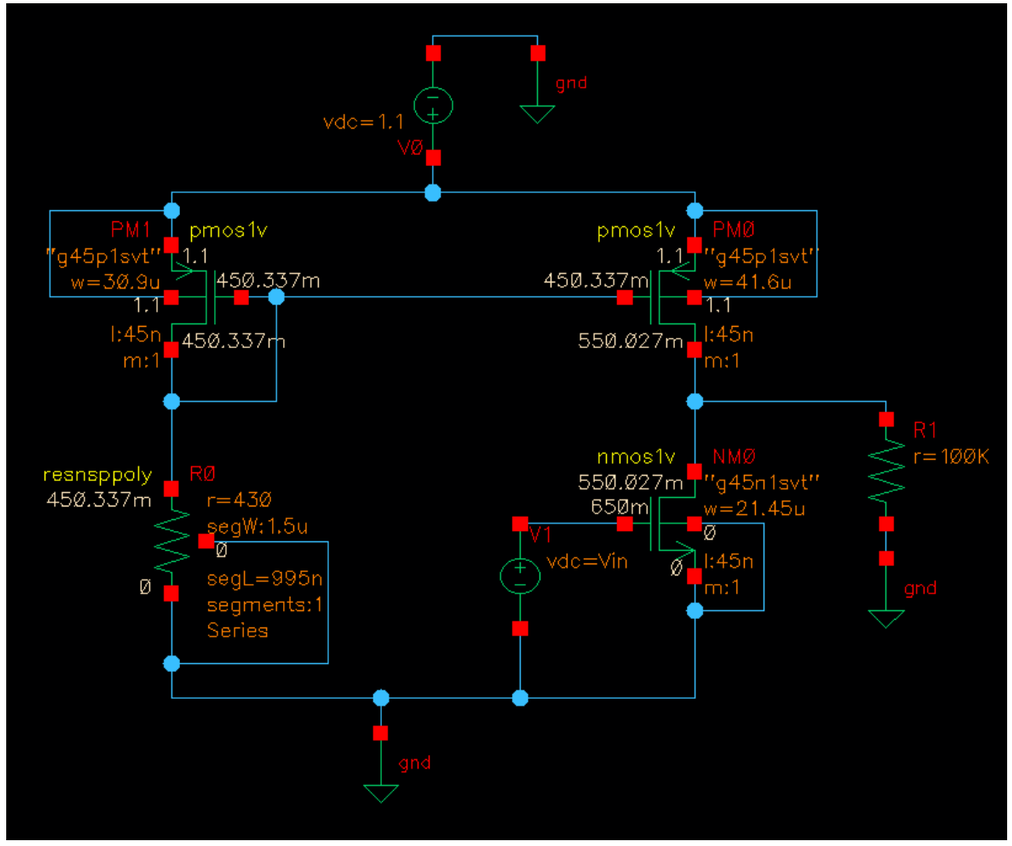
2.c. Common Source Amplifier *(continued)*

- To run DC analysis, Launch ADE Explorer and create a new view. Copy the variables from cellview (Variables → Copy From Cellview). Then set the value of **Vin** to **650 mV**.
- Now for the type of analysis, click on **Analysis → Choose → dc,** and check **Save DC Operating Point** and run the simulation.
- The values shown in the figure should be annotated on the circuit, and we can notice that our output DC voltage Vo is equal to 550 mV, which is a good value because it is approximately in the middle of the supply voltage of value 1.1 V and the ground 0 V.



- Check and Save before running the simulation.

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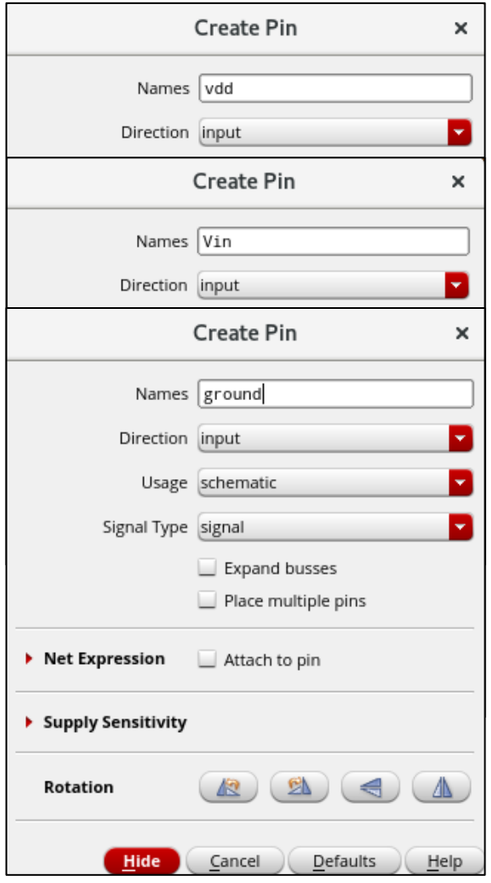
2.c. Common Source Amplifier *(continued)*

- To be able to put our schematic into a symbol we need to define input and output pins.
- To add input and output pins. Click on the **Add Pin** icon in schematic toolbar (or simply type “Ctrl + P” on your keyboard). To add the input pins on your schematic, write their names in the “Names” label, and set their “**Direction**” as “**input**”.
- Our input pins are Vin, vdd and ground.



- Give the pins meaningful names that do not contain special characters.
- Note that vdd and ground are also pins.
- Pins will become the terminals of your design.

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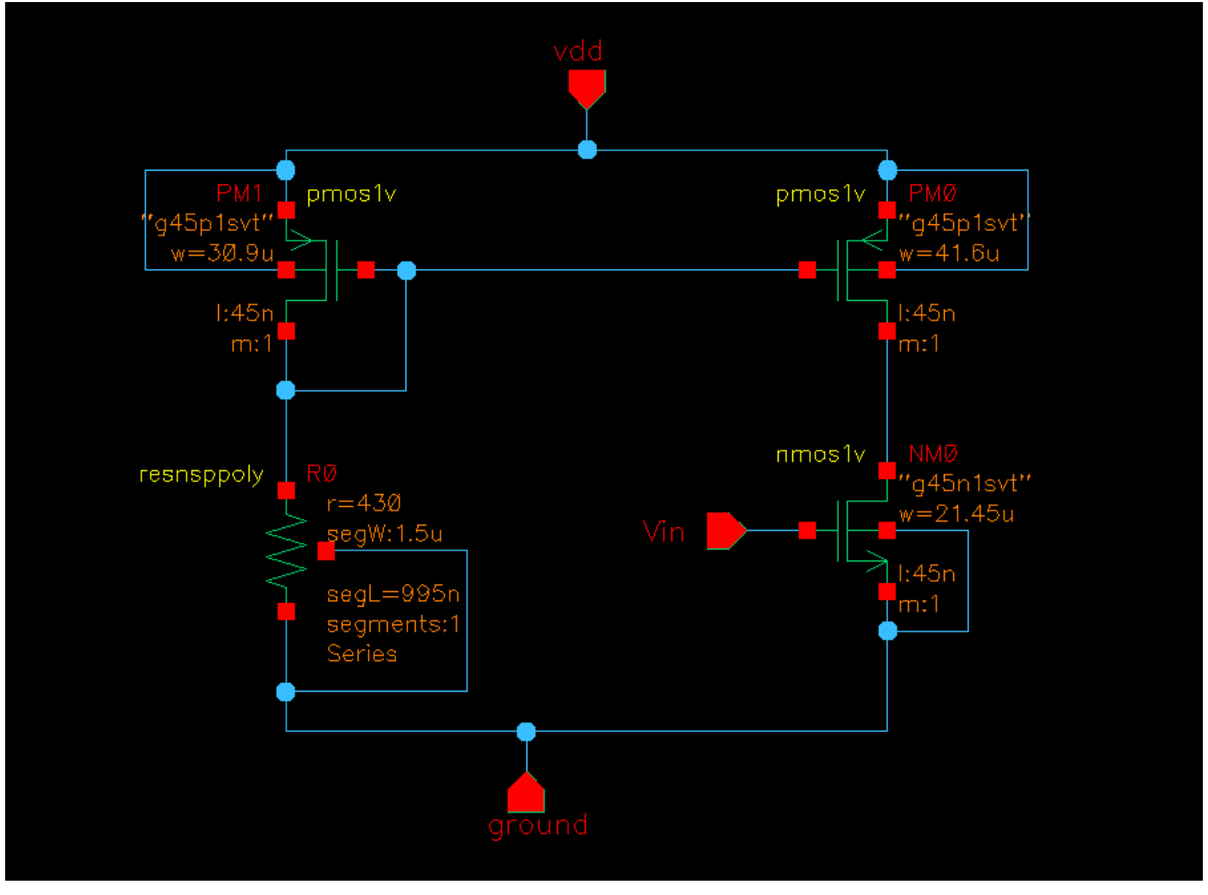
2.c. Common Source Amplifier *(continued)*

- Move your mouse pointer to the schematic, then add the input pins as shown below.



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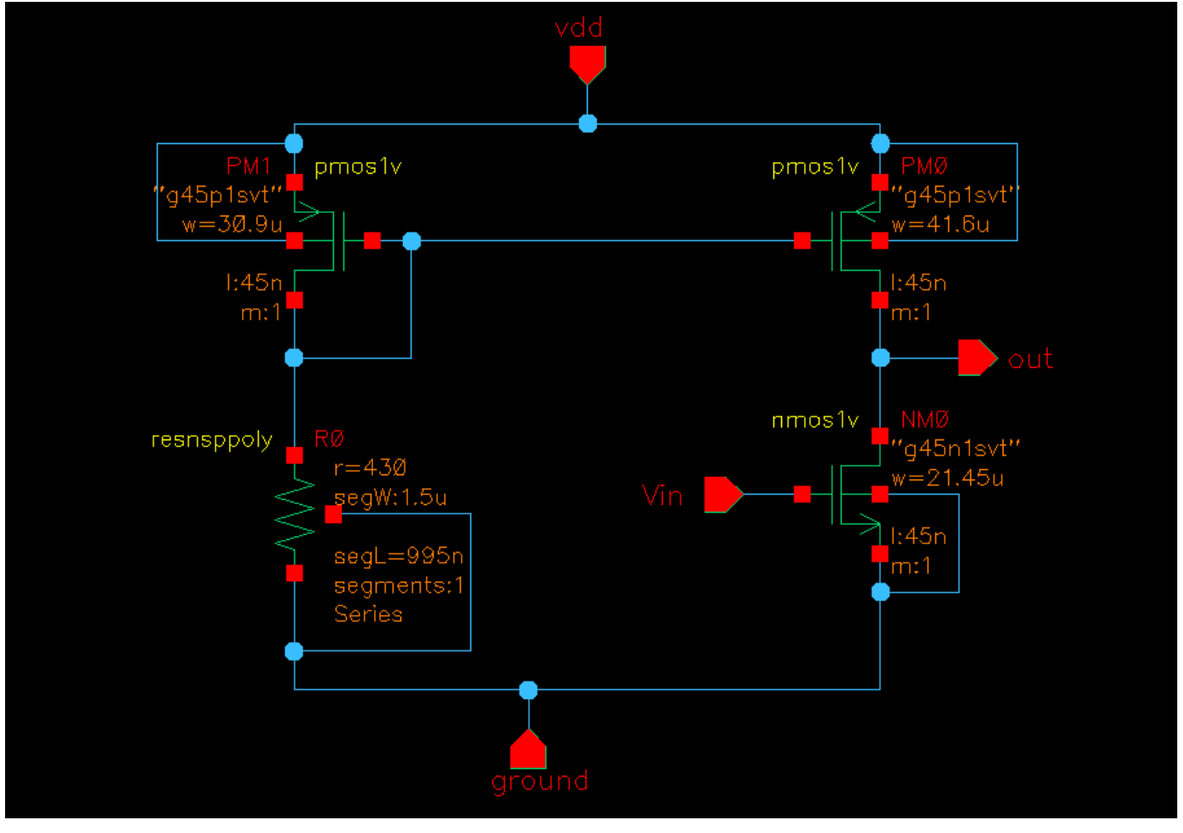
2.c. Common Source Amplifier *(continued)*

- To add the output pin, follow the same procedure used for the input pins, but make sure to set the **Direction** of the pin to "**output**".



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2.c. Common Source Amplifier *(continued)*

- Now after you have drawn your entire circuit, select “Check and Save” on the toolbar.

- If any errors occur, try to troubleshoot your drawing. (You can check your errors in the CIW).

- It is a good practice to “Check and Save” periodically using shortcuts.

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3. Creating a Symbol

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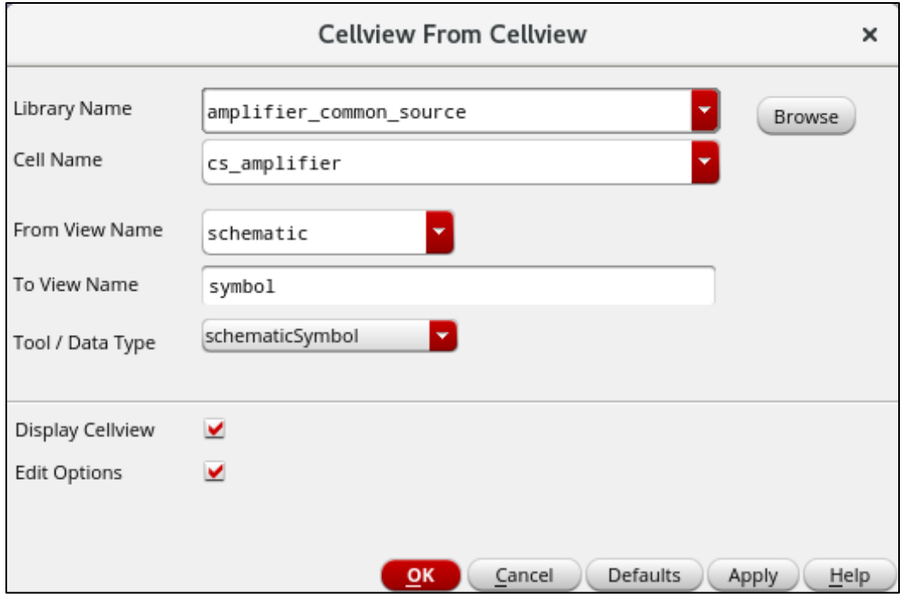
3. Creating a Symbol

- In order to use your amplifier in a test bench, you first need to create a symbol that represents it.
- In order to do that, select **Create → Cellview → From Cellview**.
- Make sure that the data is filled correctly in the window “Cellview from Cellview” form, then click **Ok**.
- Later, if a design should incorporate this one, you can use this design’s symbol view instead of its schematic view.



- Using the symbol view allows the creation of large circuits that do not look cluttered.
- For example, you have already used the symbol of a transistor in this design, without knowing exactly what it contains.

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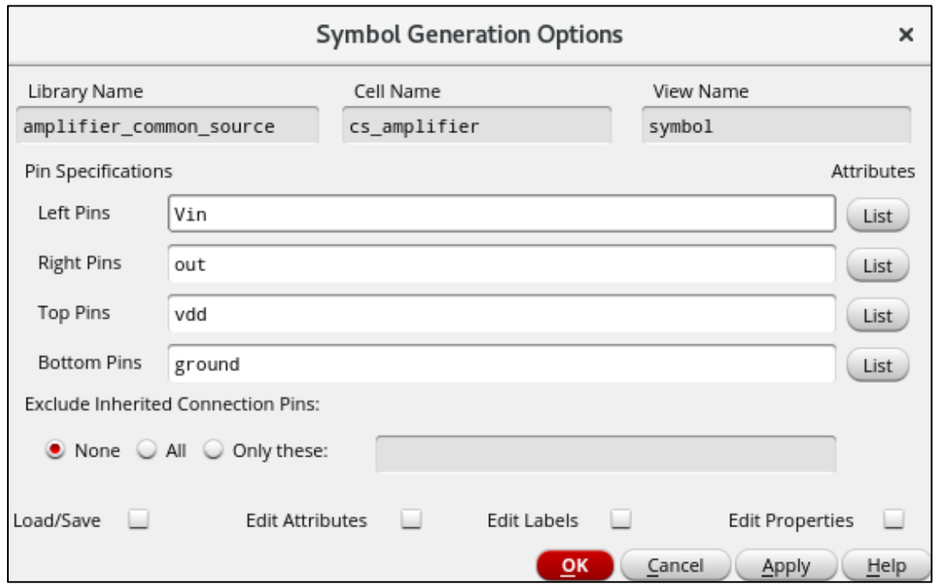
3. Creating a Symbol *(continued)*

- The “Symbol Generation Options” form pops-up, here you can customize the pin locations of the symbol generated.
- To make your design look more like an amplifier, choose the locations as shown below.



- Using the symbol views leads to what is called a hierarchical design, as opposed to a flat design.
- Due to case sensitivity, make sure you type the pin names exactly as they appear.

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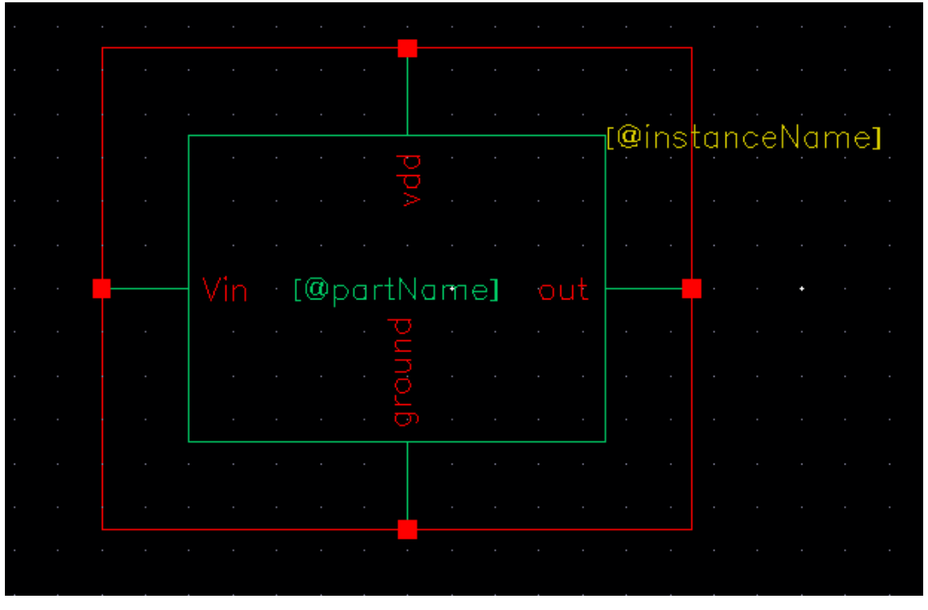
3. Creating a Symbol *(continued)*

- After choosing the locations of the pins, this is how your symbol will look like.
- To make this look more like an amplifier, it should have a triangular shape. Therefore, delete the **green** boundaries of your square, and draw a triangular shape by selecting **Create Polygon** from the toolbar.



- Some components have agreed-upon symbol shapes. For example, an amplifier is triangular.
- Ensure you click each corner individually without holding down the mouse button.

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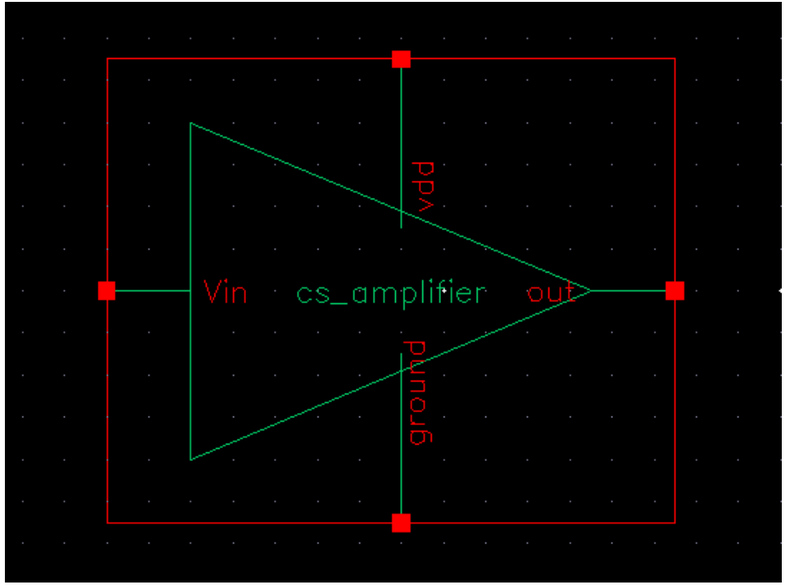
3. Creating a Symbol *(continued)*

- After you have drawn a triangular shape, your symbol should look as shown below.
- Extend the connections at the vdd and ground by clicking on the edge of the connection once and extending it.
- The pointer should look like this. 
- You can also change the “@partName” to “cs_amplifier”.



- Don’t forget to check and save before exiting.

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4. Test Bench

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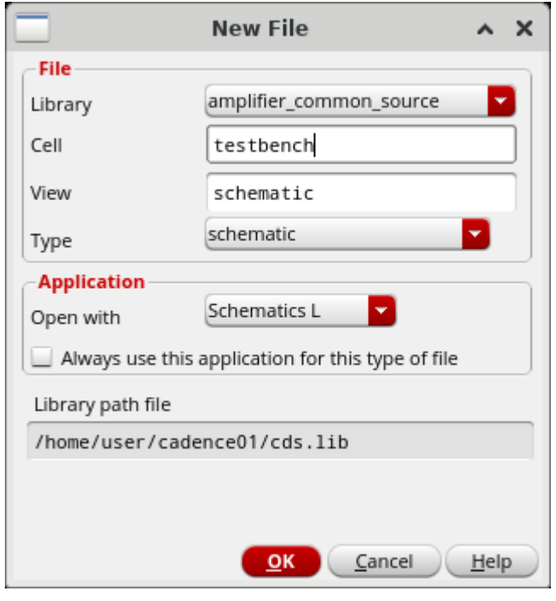
4. Test Bench

- The purpose behind creating a symbol for a schematic is to use it in a test bench, therefore we should create a new Schematic Cell View.
- From the Library Manager, click on our Library, then select **File → New → Cell View**.



- The test bench is yet another schematic that incorporates the symbol view of the design (amplifier).
- The test bench is distinguished from the design itself much like in a laboratory setup.

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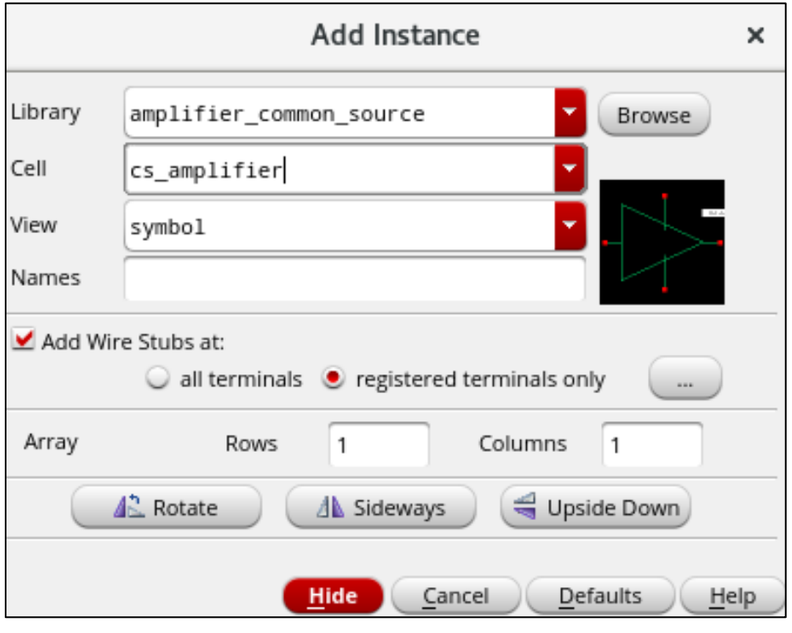
4. Test Bench *(continued)*

- To start creating our test bench circuit, we need to add the amplifier symbol we generated previously.
- Add the amplifier symbol in the schematic, by pressing ‘I’ on your keyboard, and then select it from the “amplifier_common_source” library as shown.



- It is a good practice to distinguish the test bench from the design. For example, one design might be tested in several different test benches. Also, one test bench might be built for different designs.

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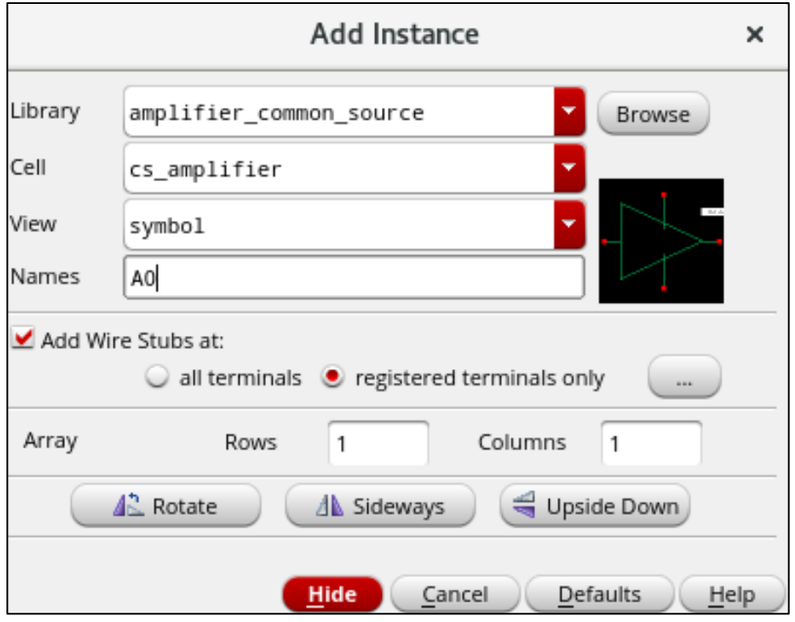
- Library
- NMOS
- PMOS
- CS Amplifier
- Symbol
- Test Bench

4. Test Bench *(continued)*

- Name your amplifier ‘A0’ as shown below.
- Move your mouse pointer to position it in your test bench schematic.



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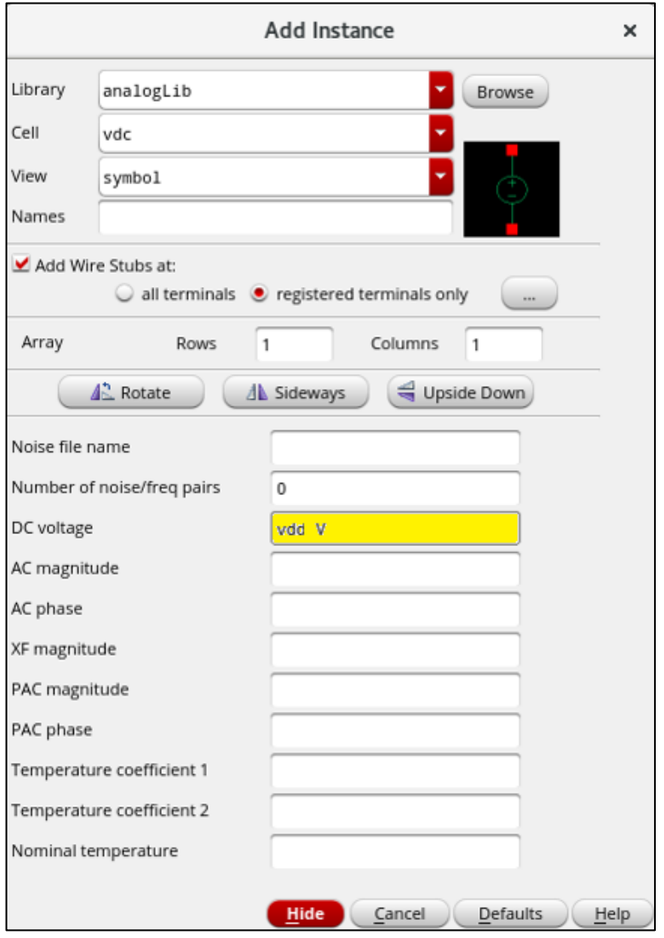
4. Test Bench *(continued)*

- First, the amplifier should be provided with a supply voltage.
- To provide this supply, add the vdc sources to your schematic from the analog library (analogLib).
- Set the DC voltage of the vdc source to **vdd**.
- Add a ground from the analogLib library.
- Connect the voltage source and the ground as shown in the next slide.



- For information regarding any of the other parameters, check the help files.

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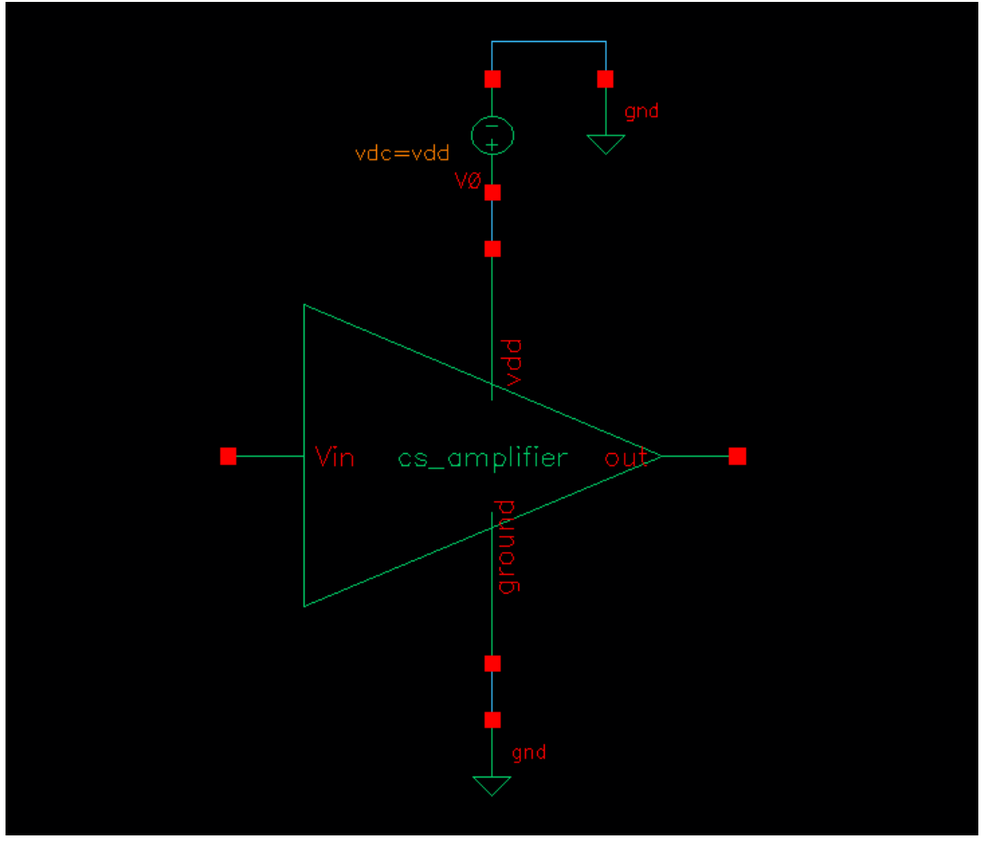
- Library
- NMOS
- PMOS
- CS Amplifier
- Symbol
- **Test Bench**

4. Test Bench *(continued)*

- So far, the circuit should look like this;



- Don't forget to flip the voltage source.

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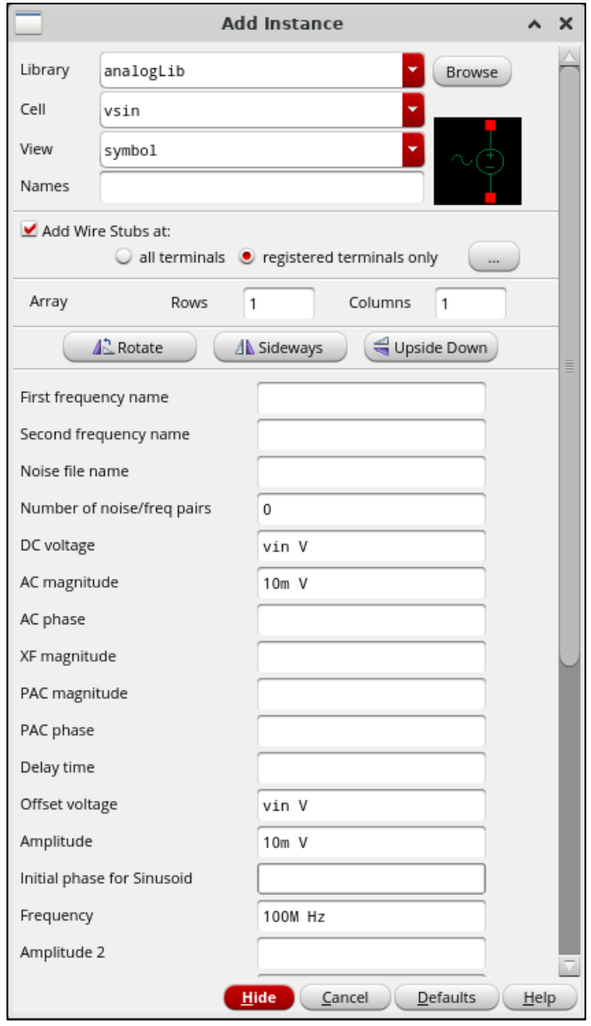
- Library
- NMOS
- PMOS
- CS Amplifier
- Symbol
- **Test Bench**

4. Test Bench *(continued)*

- To complete the test bench schematic, add the input voltage, and the load at the output.
- First, add an input voltage, select “vsin” from the analogLib library with the following properties:
  - DC voltage = Offset Voltage = vin V
  - AC magnitude = Amplitude = 10 mV
  - Frequency = 100 MHz



- When adding a vsin source, the DC voltage and the Offset voltage should be the same and this applies also to the AC magnitude and Amplitude.
- One of them is for Transient analysis and the other for AC analysis.

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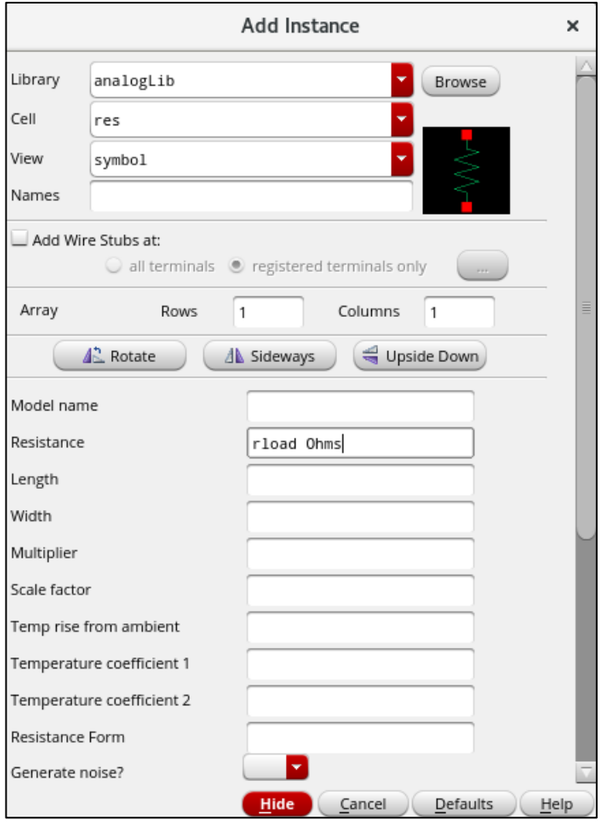
- Library
- NMOS
- PMOS
- CS Amplifier
- Symbol
- **Test Bench**

4. Test Bench *(continued)*

- Add a resistor with the following properties as a load on the output terminal.



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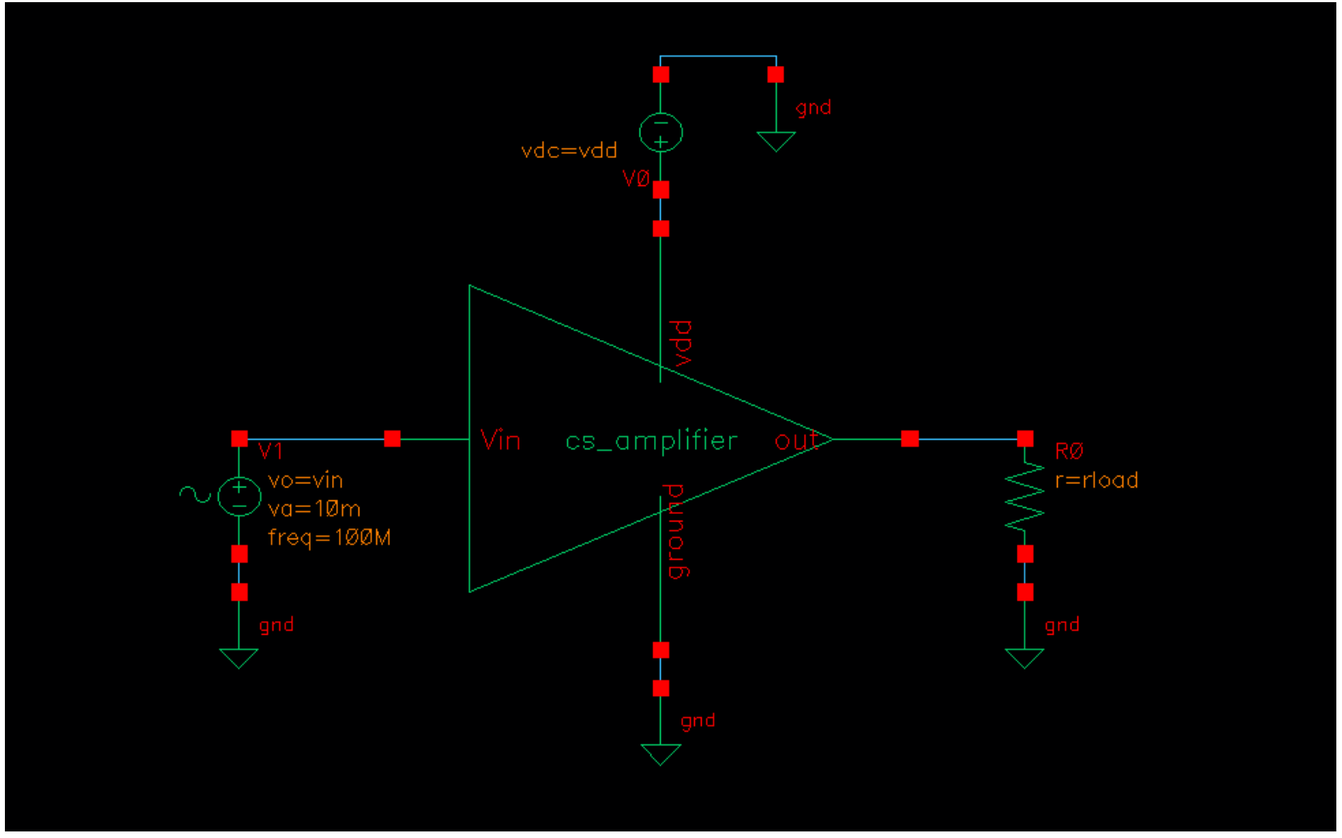
- Library
- NMOS
- PMOS
- CS Amplifier
- Symbol
- **Test Bench**

4. Test Bench *(continued)*

- Connect the circuit as shown below.



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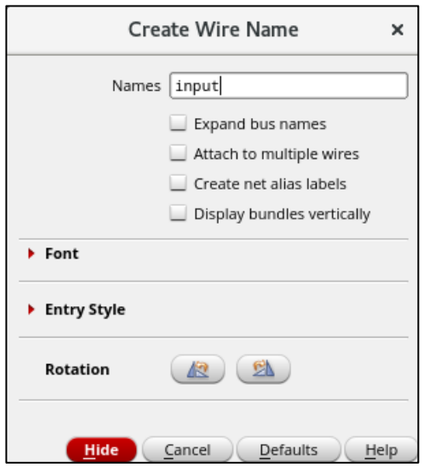
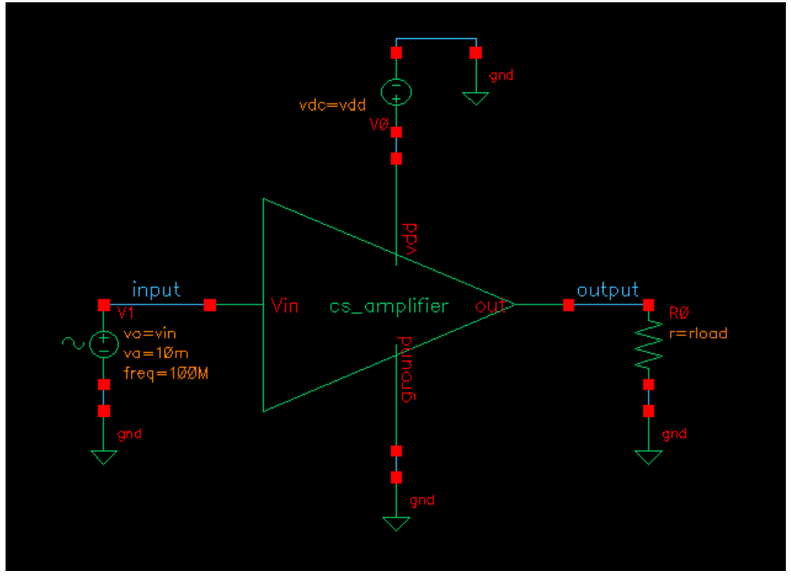
4. Test Bench *(continued)*

- We will also name the input and output connections; this will help later to easily identify the waveforms.
- Click on **Create → Wire Name…** (or simply type ‘L’ on your keyboard).
- Then attach the labels by clicking on the corresponding connections as shown below.
- Click on “Check and Save” on the toolbar to save your work and check for errors.





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