Virtuoso 23.1
Module 8 - Layout

American University of Beirut (AUB)
Lebanon

Contents

Module Objective

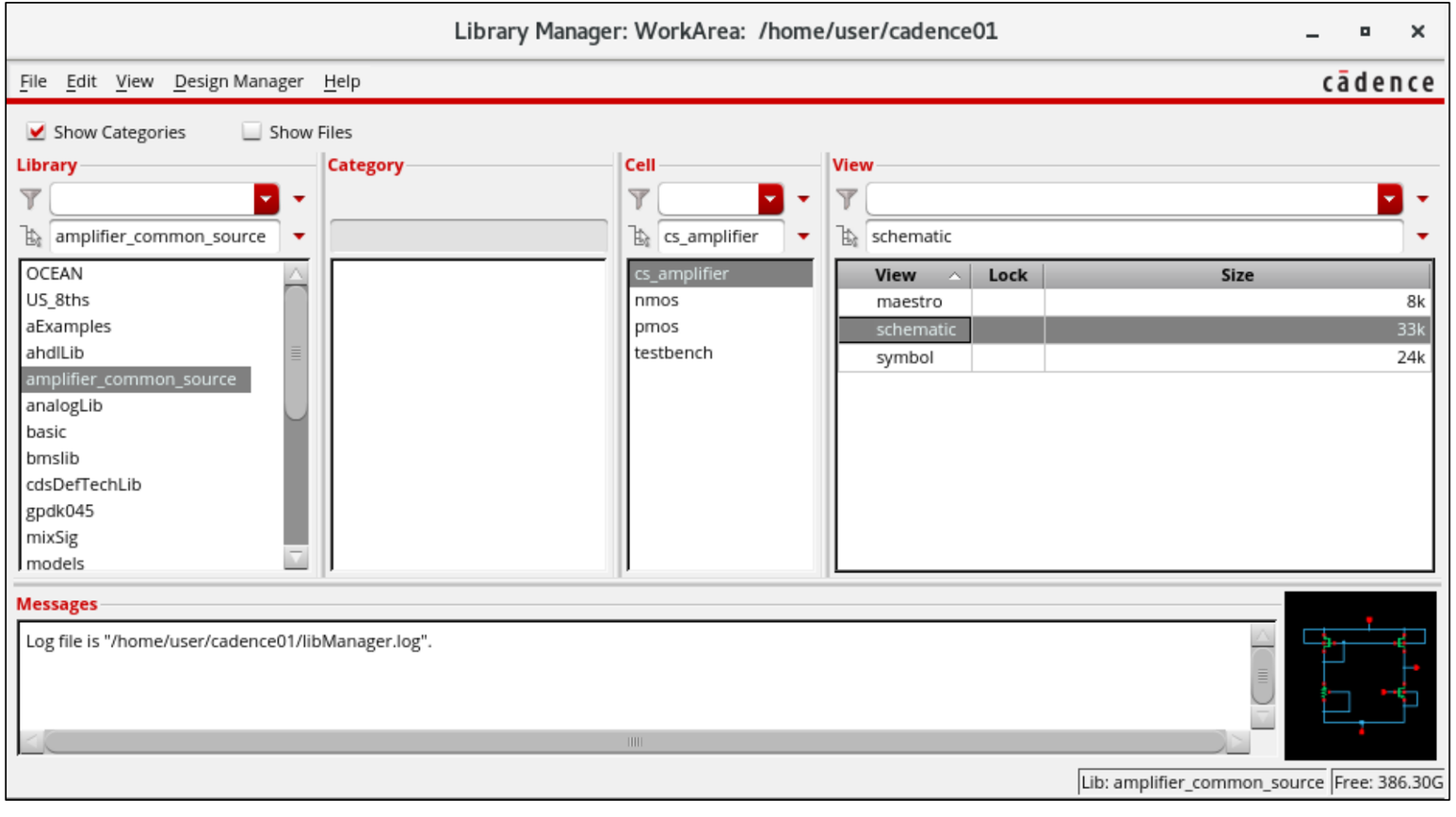
In this module, we will learn how to:

- add the dummy devices and understand the purpose of the dummies
- place the devices in a way to achieve less overall area
- draw the bulk of the transistors
- connect the components using different metal layers

1. Adding Dummy Transistors

1. Adding Dummy Transistors

- From the Library Manager, open the **schematic** view of the cs_amplifier cell.



cadence

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- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

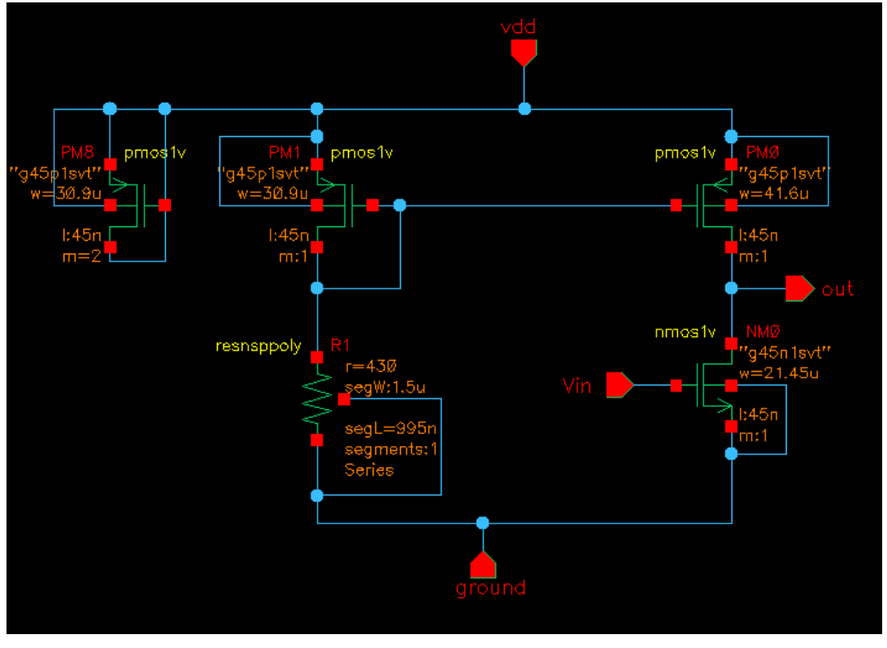
1. Adding Dummy Transistors *(continued)*

- In general, all the devices have to be “matched” in order to have a layout that meets the specifications.
- Layout Design Engineers use different techniques to make the devices matched in a design.
- One of the methods used is the addition of “dummy” devices. These devices are not part of the design (in our case the CS Amplifier). When used correctly they influence the performance of the circuit, meaning our specifications are most likely to be passed (however this is not guaranteed).
- According to the placement of the main devices that are part of the design, the number of dummy devices are differed.
- In our case, we will add 6 dummy transistors and 2 dummy resistors.
- First, we have to modify the schematic by adding the dummy devices.
- In case of a transistor, a dummy must have the same width and length.

cadence

1. Adding Dummy Transistors *(continued)*

- Select the left PMOS transistor. To copy the transistor, either right click and choose Copy or use the bindkey C.
- The connections of the Gate, Source, Drain, and Bulk are connected to vdd.
- Place and wire the copied transistor as shown in the figure.



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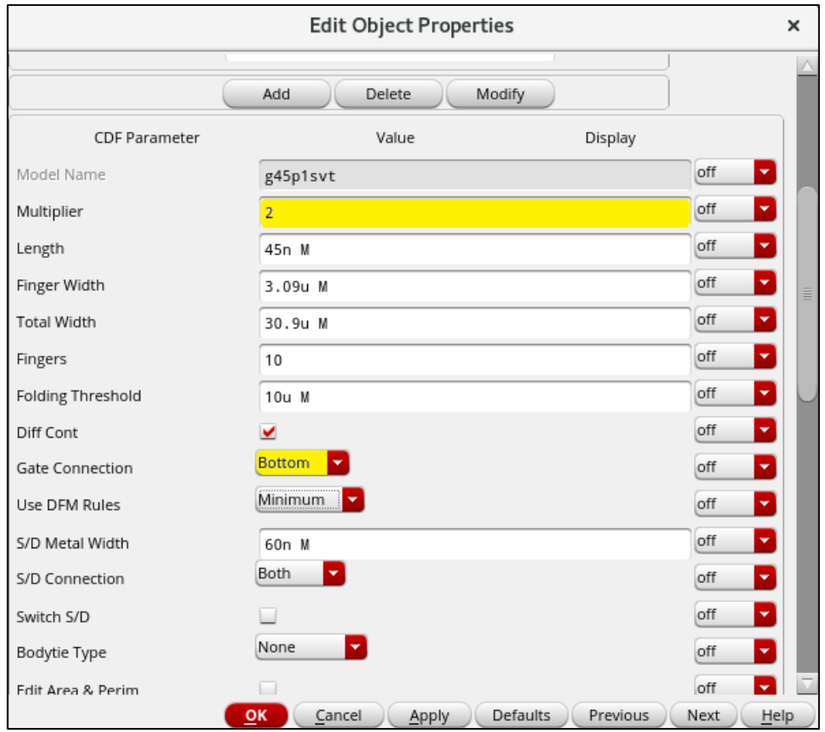
- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

1. Adding Dummy Transistors *(continued)*

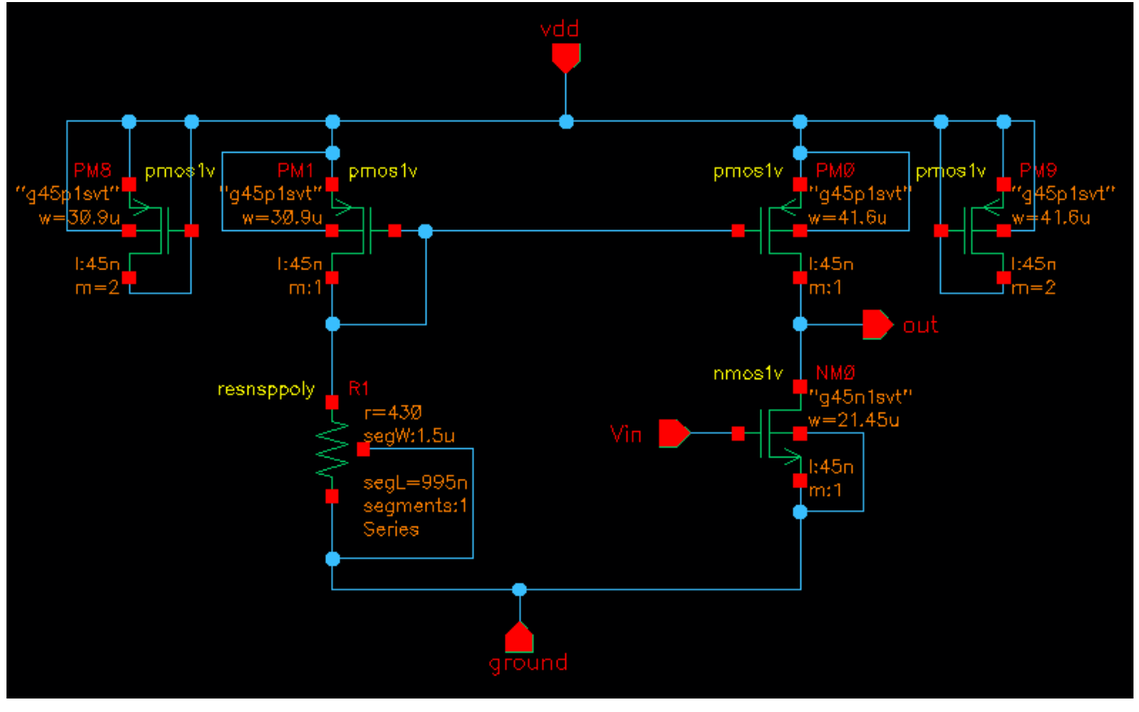
- Select the copied transistor, and press Q to open the Edit Object Properties.
- Change the **Gate Connection** to **Bottom** and the **Multiplier** to **2**.
- Make sure the S/D Connection is set to Both.

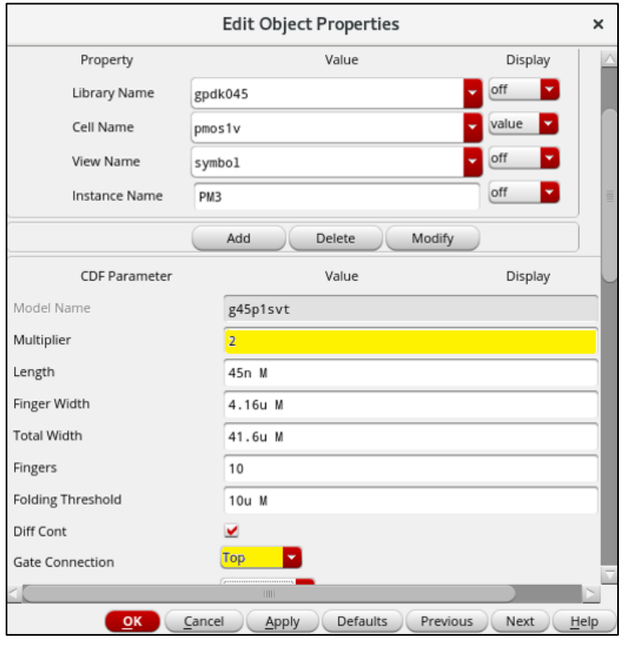


cadence

1. Adding Dummy Transistors *(continued)*

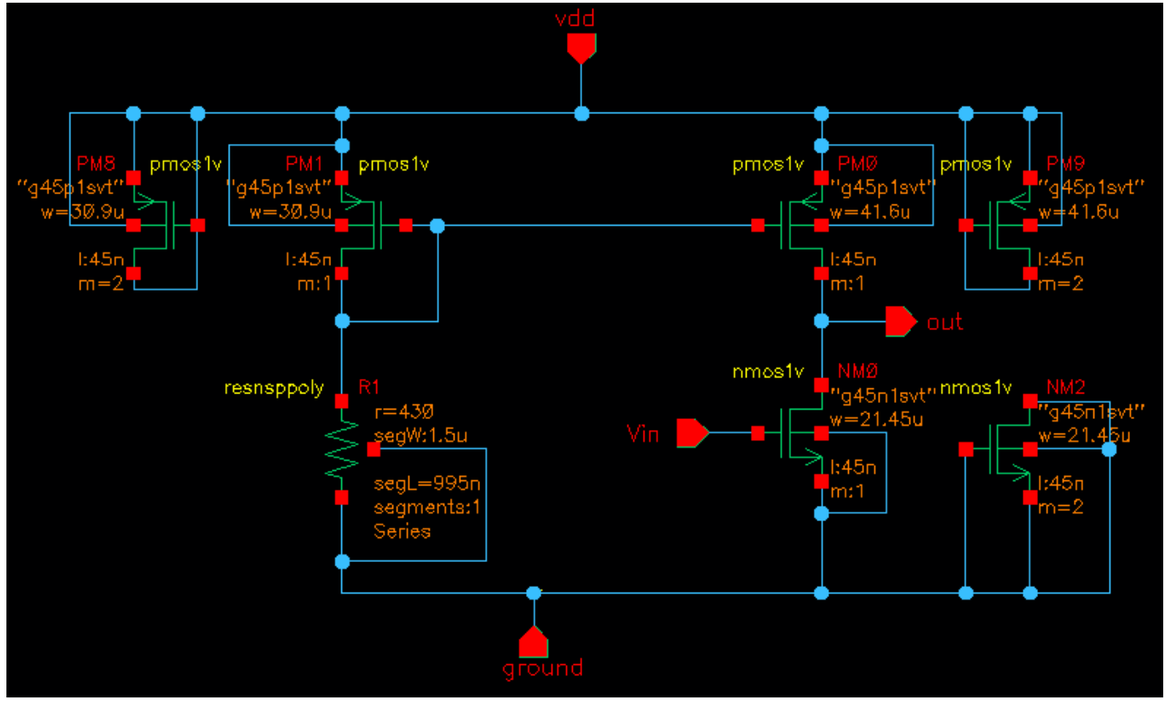
- Select the right PMOS transistor, copy, and wire it as shown in the figure below.
- Also, select the copied transistor and change the **Gate Connection** to **Top**, the **Multiplier** to **2**, and make sure the S/D Connection is set to Both.

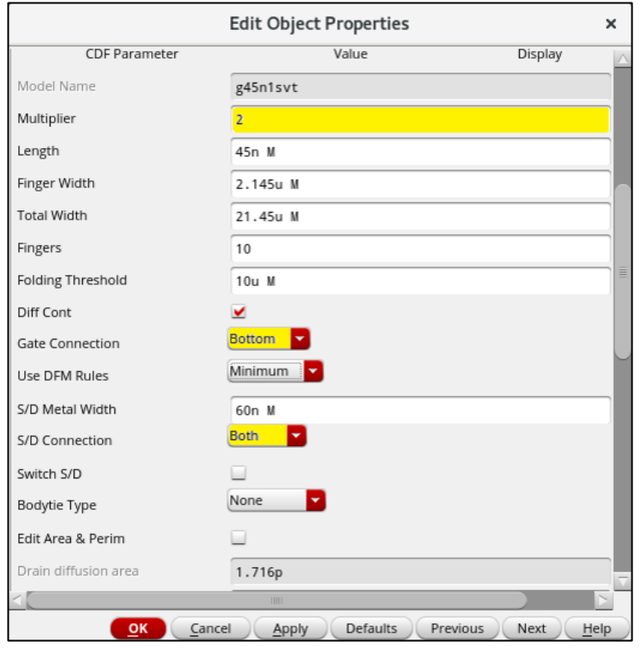




1. Adding Dummy Transistors *(continued)*

- Select the NMOS transistor, copy, and wire it as shown in the figure below.
- Also, select the copied transistor and change the **Multiplier** to **2**. Make sure the Gate Connection is set to Bottom, and the S/D Connection to Both.





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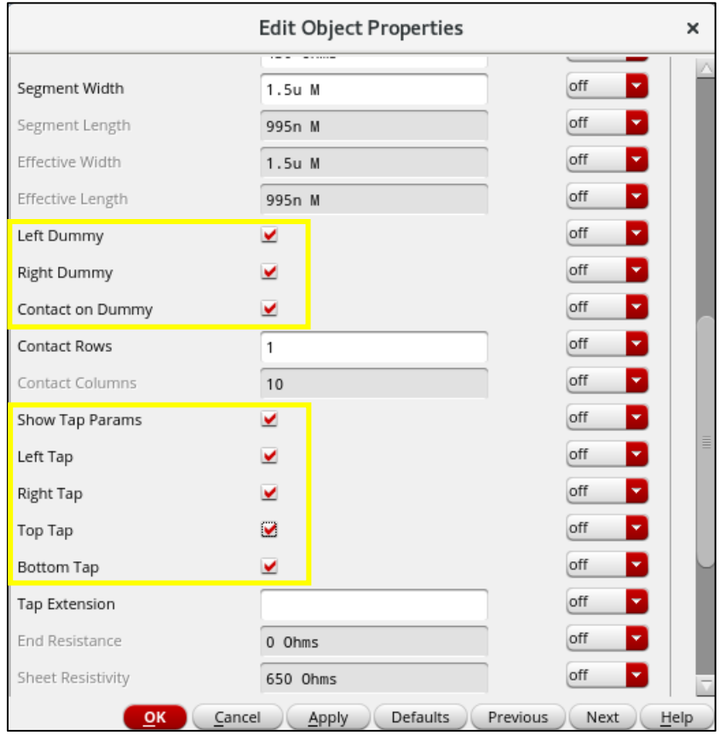
1. Adding Dummy Transistors *(continued)*

- Select the resistor and open the Edit Object Properties form.
- Make sure to select the checkbox of all the parameters shown in the figure below. Click OK.
- **Check and Save the schematic.**



- Note that enabling **Left Dummy** and **Show Tap Params** will cause the parameters to appear if they are not already displayed.

2. Layout MXL Overview

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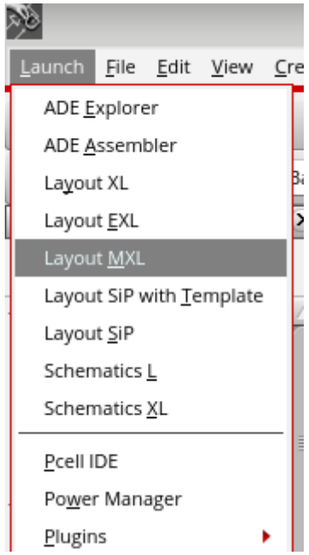
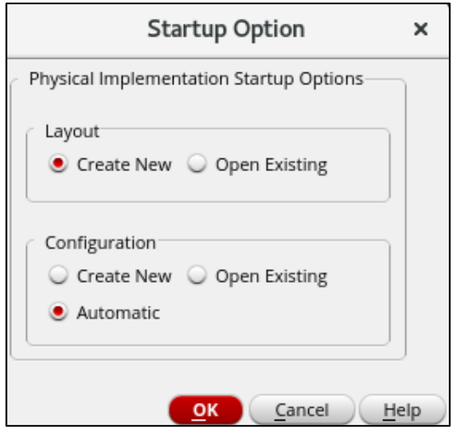
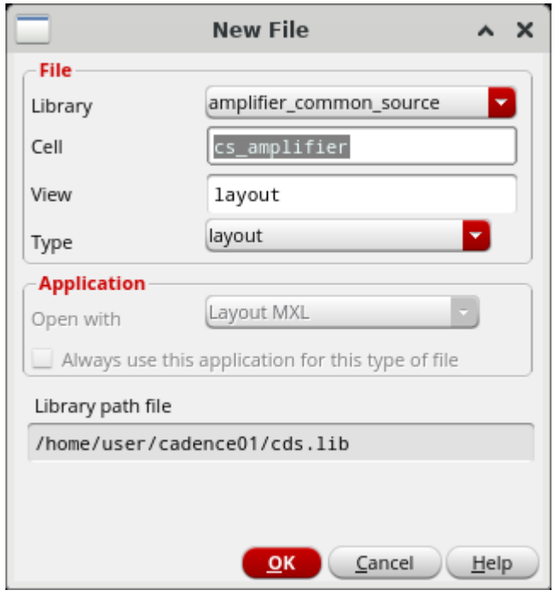
- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

2. Layout MXL Overview

- Before designing the common source amplifier, it is important to explore the tool Layout MXL to be acquainted with the toolbar and the features.
- Under **Launch**, click on **Layout MXL**.
- The Startup Option will pop-up, click **OK** to proceed.
- The New File form will pop-up, click **OK** to Launch the **Virtuoso Layout MXL.**







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- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
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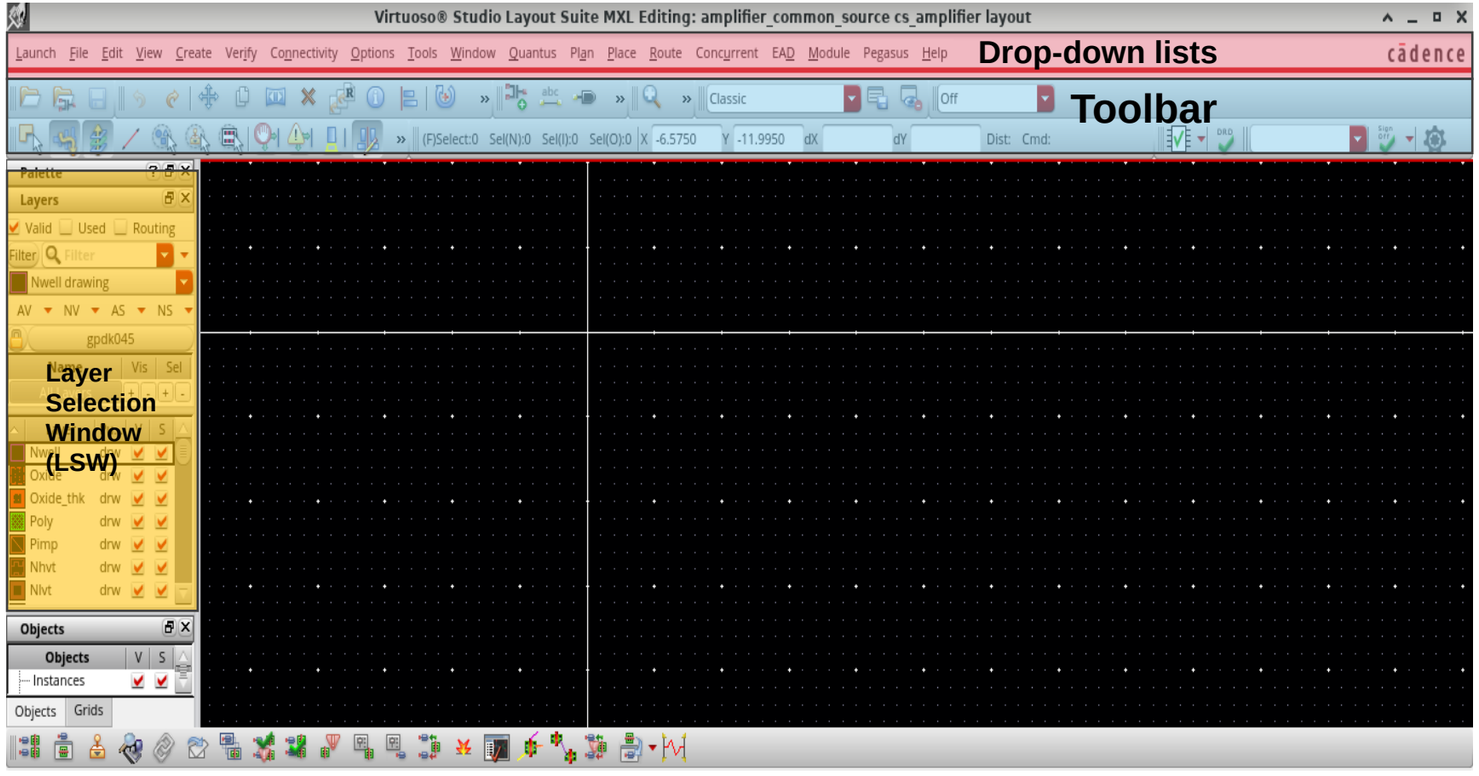
- Routing the Components

2. Layout MXL Overview *(continued)*

- The black canvas is where we will place the components and wire them using the metal layers from the Layer Selection Window (LSW).



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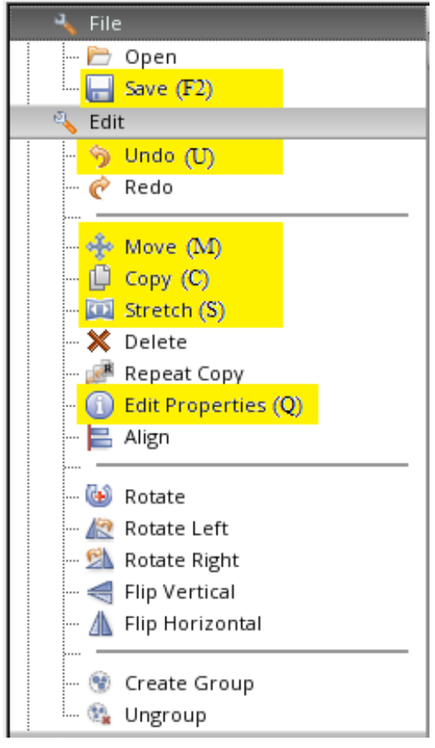
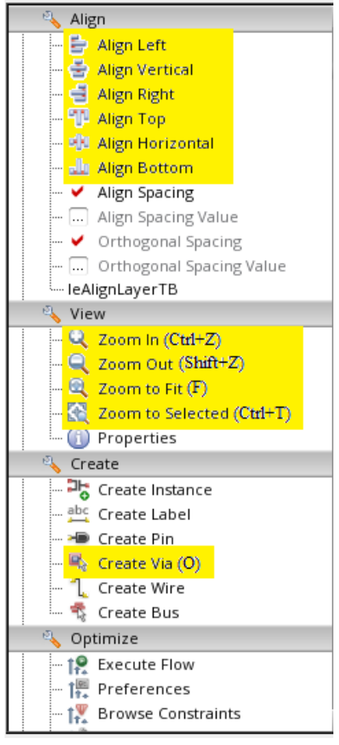
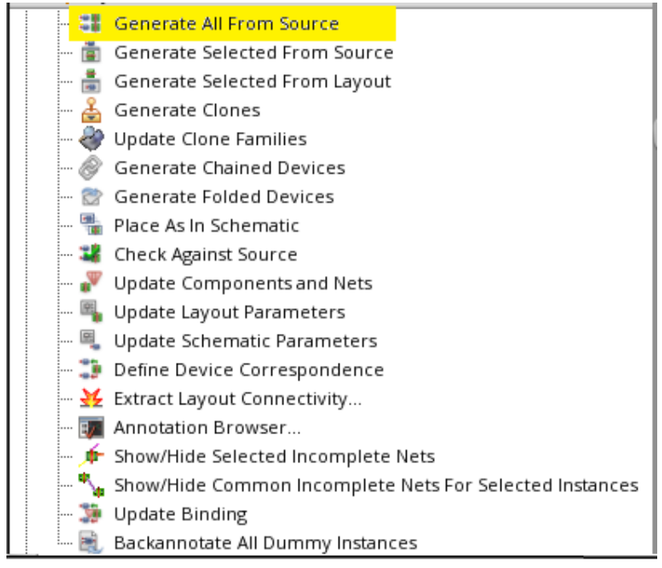
2. Layout MXL Overview *(continued)*

- Below are some of the most frequently used features:



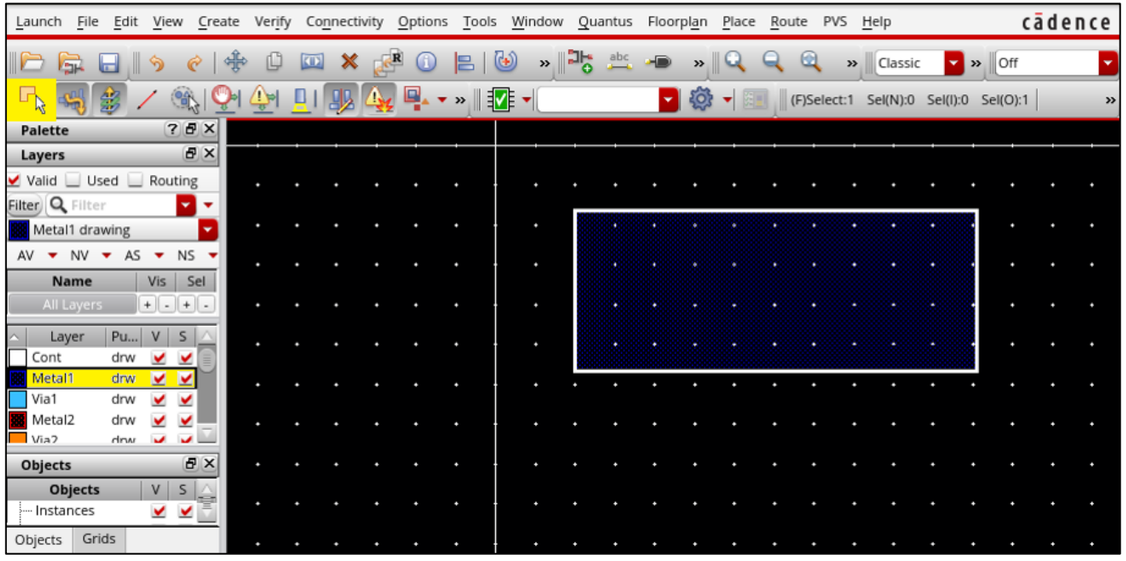




- Note that you can add the Align feature in the Toolbar. From the drop-down list of Window, select Toolbars → Align.

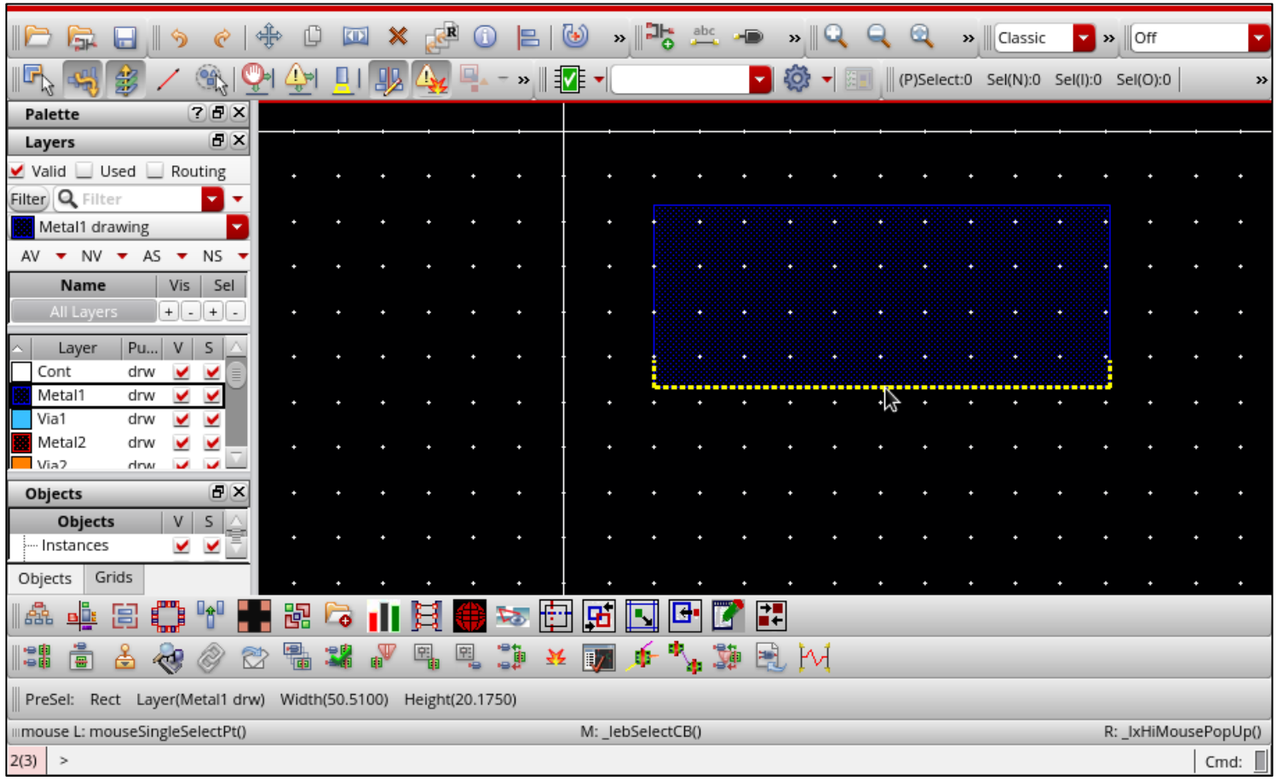
2. Layout MXL Overview *(continued)*

- We will draw a rectangle and learn how to adjust the size by using the Full Select and Partial Select features from the Toolbar.
- Select Metal1 from the LSW.
- From the drop-down list of Create, select Shape → Rectangle (or use the bindkey R).
- Draw a rectangle of any size.
- Notice when you select the rectangle, all the edges of the rectangle are selected. This is because we are in the Full Select mode. Notice in the toolbar the icon  .



2. Layout MXL Overview *(continued)*

- Click on the icon Full Select  once to change the mode to Partial Select  .
- Now if you hover over the rectangle, you can notice that you are able to select an edge.



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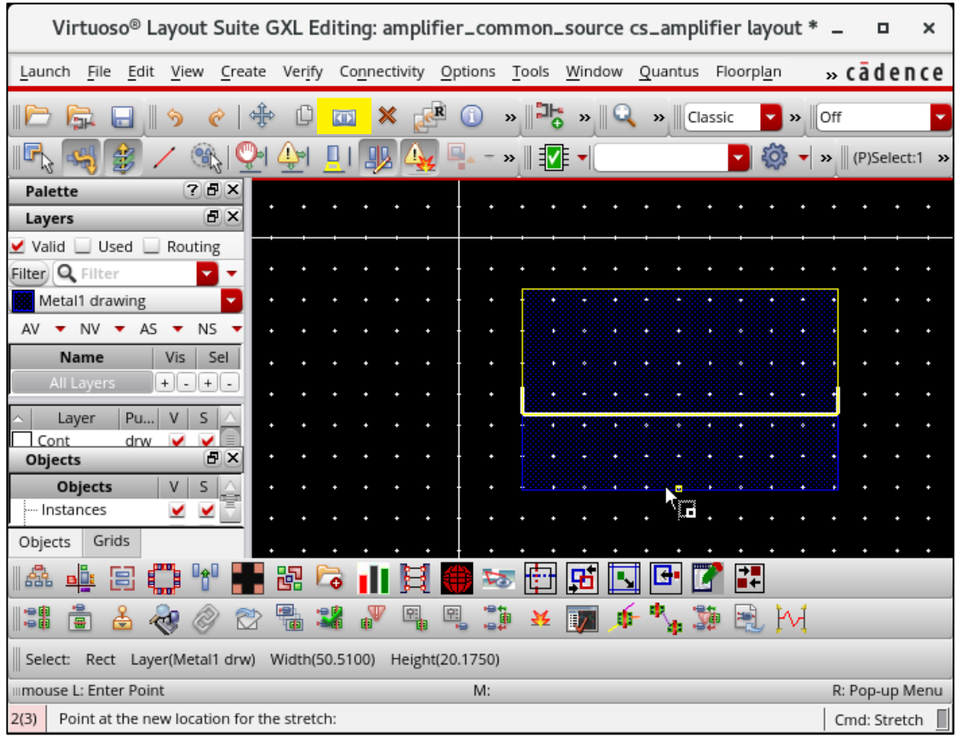
- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

2. Layout MXL Overview *(continued)*

- Click on the icon  from the Toolbar to Stretch the rectangle.
- You can also choose Edit → Stretch or use the bindkey S.
- Click on an edge once and move the mouse pointer to adjust the rectangle.
- Left-click to confirm the modification (or press Enter).



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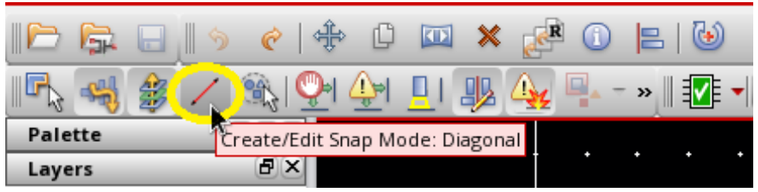
2. Layout MXL Overview *(continued)*

- Another important feature is the Create/Edit Snap Mode.



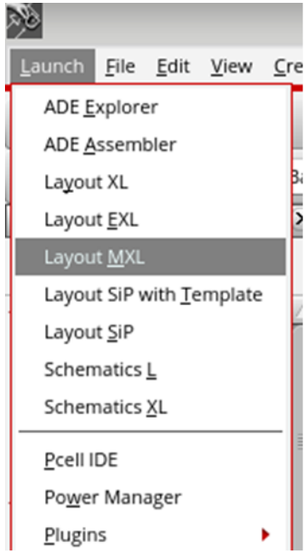
- There are three choices:
  - Diagonal 
  - Any Angle 
  - Orthogonal 
- Click on the icon  to change the mode.
- Click on the icon Move  from the Toolbar (Edit → Move or bindkey M).
- Select the rectangle and try to move it by changing the Snap Mode.
- Notice when Diagonal is selected, the rectangle moves diagonally, up, down, left, and right.
- When Any Angle is selected, the rectangle moves in any angle on the canvas.
- When Orthogonal is selected, the rectangle moves up, down, left, and right.
- **Close the Layout view without saving.**

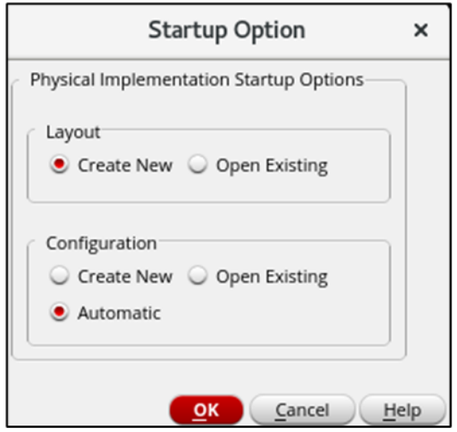
cadence

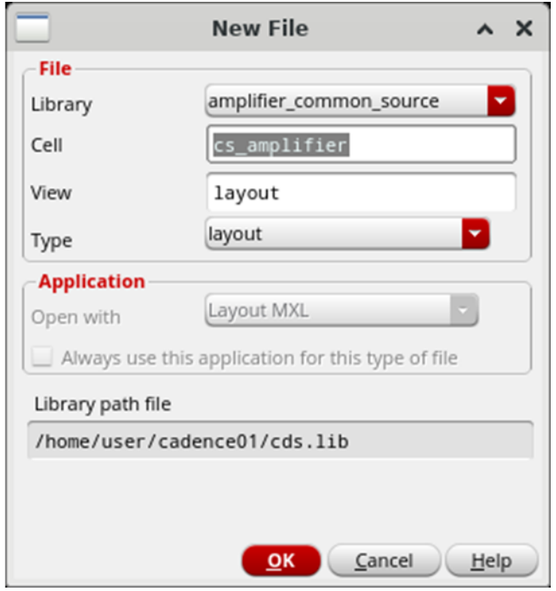
3. Generating the Components

3. Generating the Components

- Open the **schematic view** of the **cs_amplifier cell**.
- Under **Launch**, click on **Layout MXL**.
- The Startup Option opens, click OK to proceed.
- The New File form opens, click OK to Launch **Virtuoso Layout MXL.**



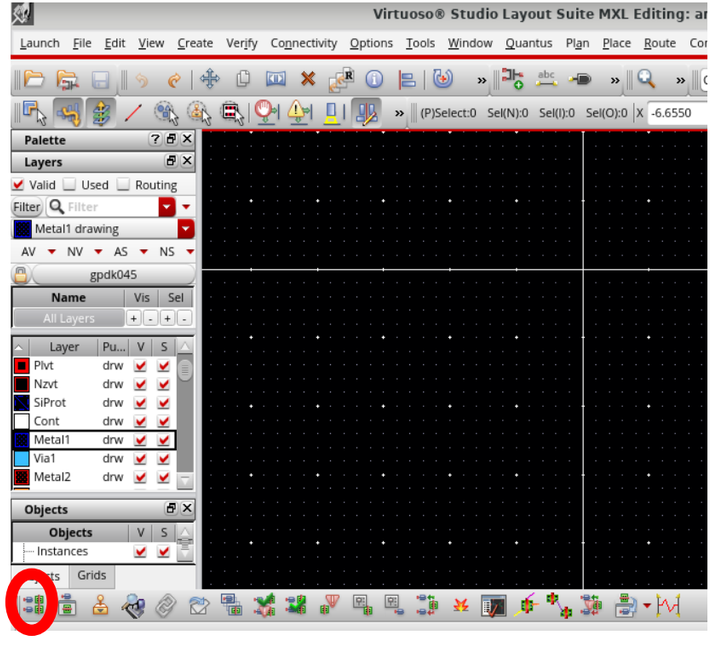


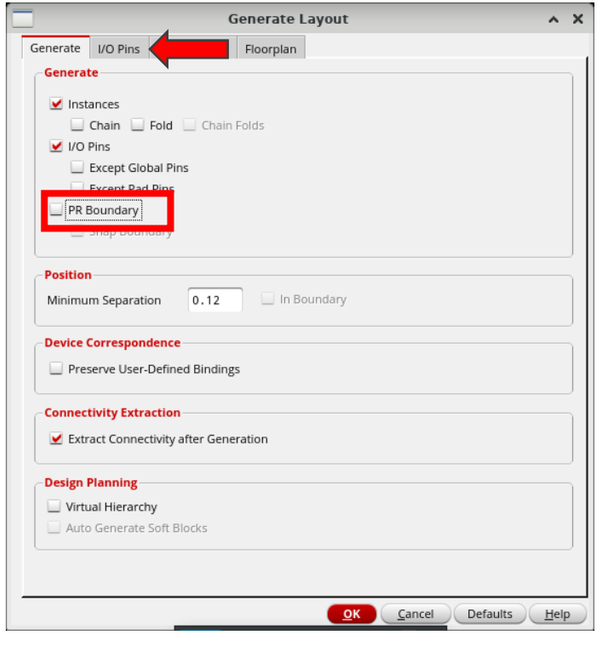


cadence

3. Generating the Components *(continued)*

- We need to generate the components from the schematic.
- Click on the **Generate All From Source** icon located at the bottom left.
- If you received the message “This command will delete all constraints, wiring and instances in 'amplifier_common_source cs_amplifier layout'. It cannot be undone. Continue?”, **click Yes to proceed**. This message means you had previously saved the rectangle that we drew while exploring the tool.
- The Generate Layout window opens, uncheck the PR Boundary and click on the I/O Pins tab.



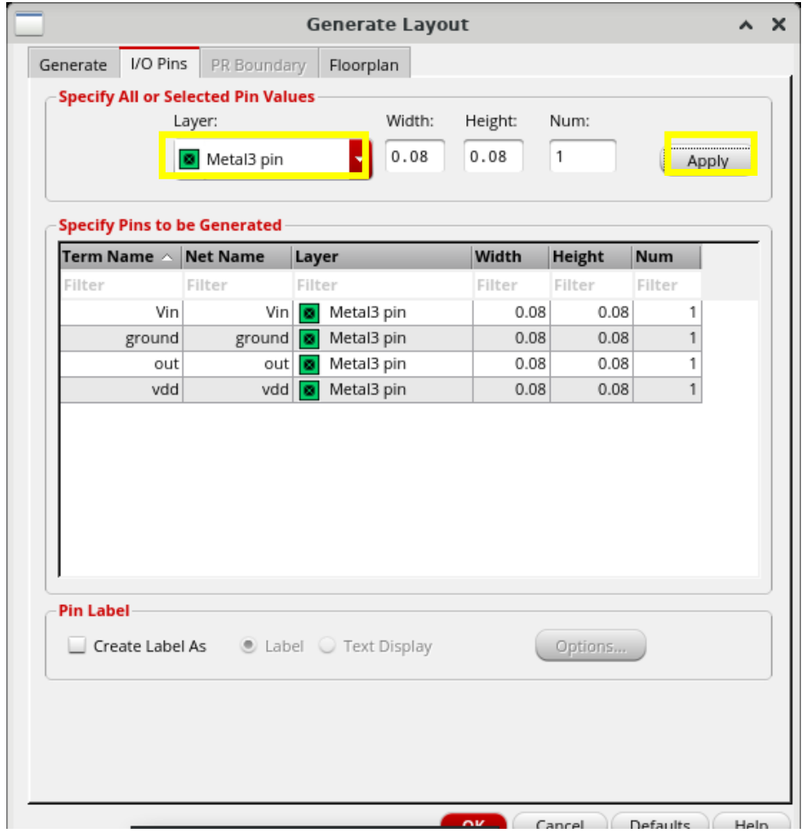


- The black window of the layout is where we will be placing the components and connecting them.

cadence

3. Generating the Components *(continued)*

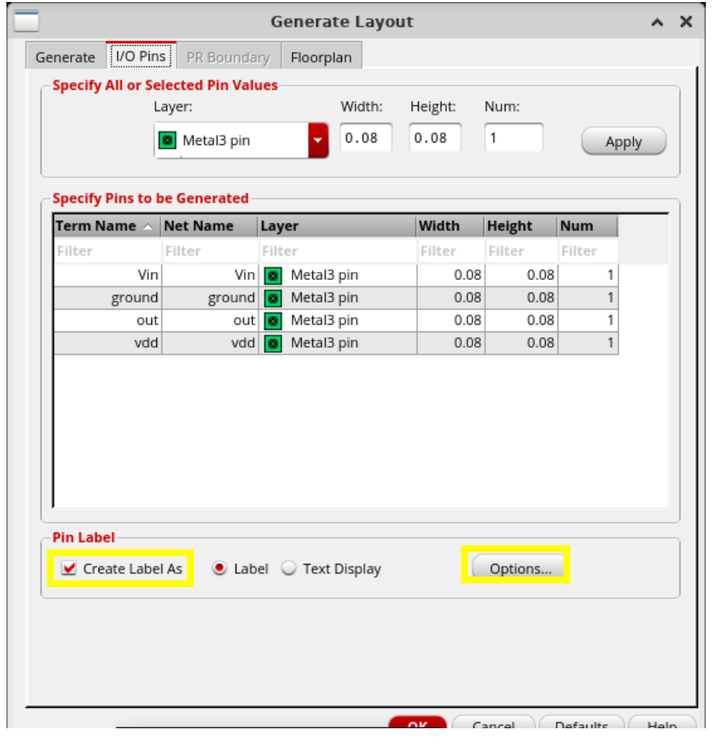
- Change the Layer to “Metal3 pin” from the drop-down list and click on Apply.
- Notice that the Layer column for all the pins is now of the type “Metal3 pin”.

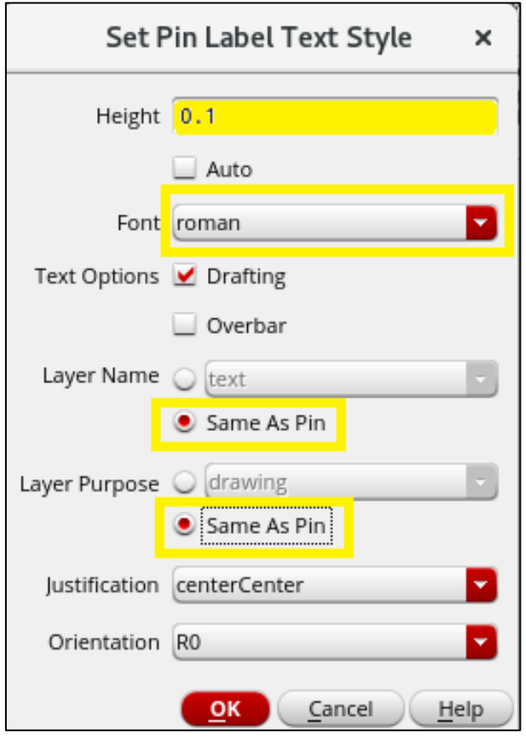


- We must change the Layer of each pin according to the connection Layer it will be in contact with. Also, we must change it to “pin”, otherwise we will encounter errors later when we run the Physical Verification Systems.

3. Generating the Components *(continued)*

- Select “Create Label As”, choose “Label”, and click on **Options**.
- Change the “Set Pin Label Text Style” form as shown in the figure.
- Click OK to close the Set Pin Label Text Style form and the Generate Layout form.





- Note that it is important for the Label to have the same Layer as that of the pin, otherwise we will encounter errors when we run the Physical Verification Systems.

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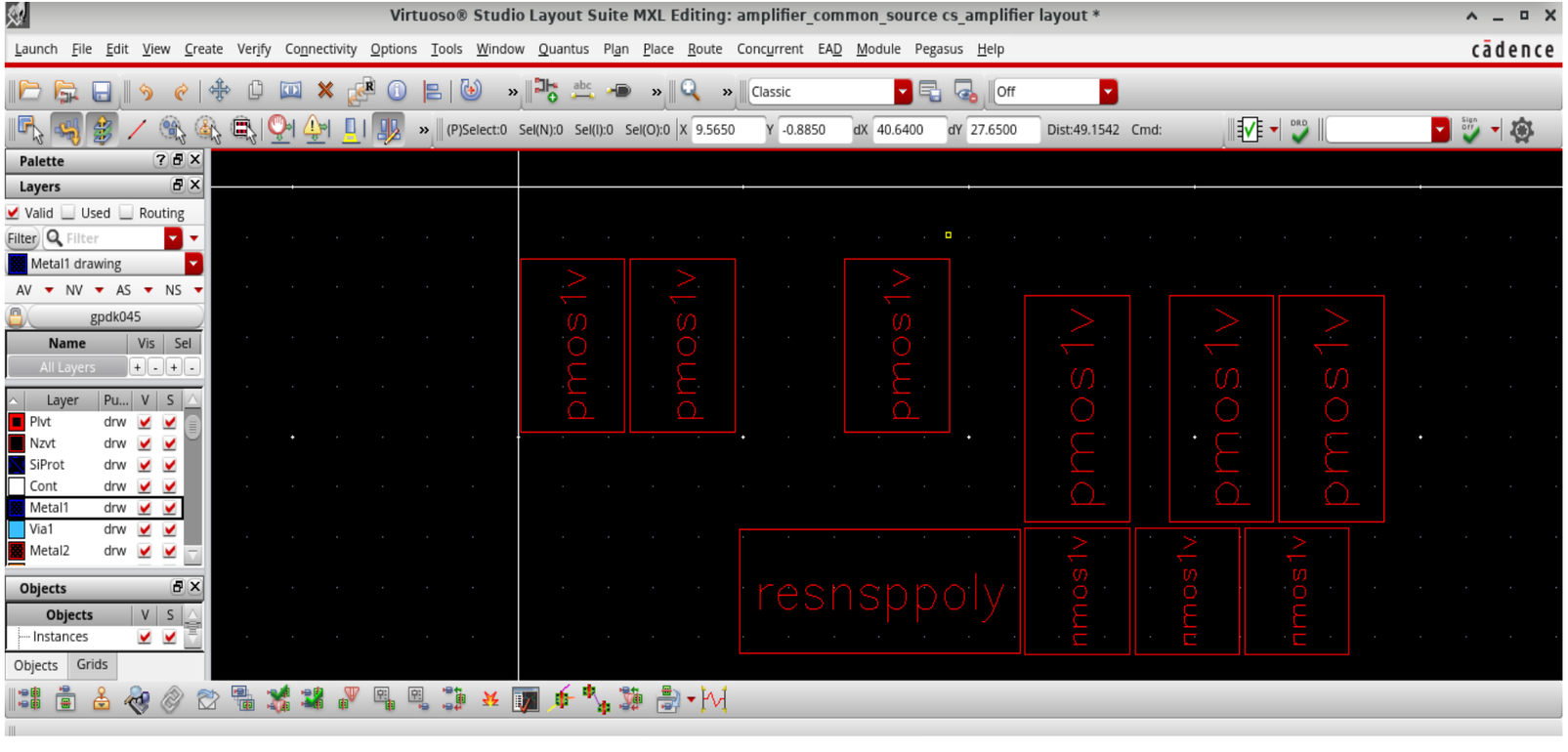
3. Generating the Components *(continued)*

- The components are now generated and placed as shown in the figure below.
- The pins are located at the top left of the canvas.



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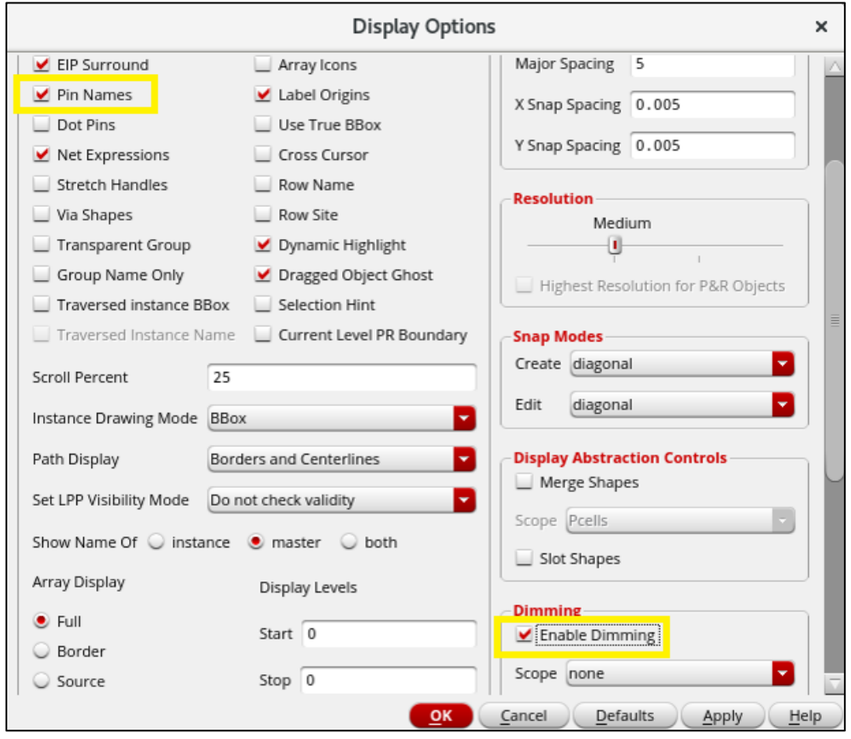
3. Generating the Components *(continued)*

- Select from the toolbar, Options → Display (or simply press E on the keyboard).
- Enable Pin Names and Enable Dimming.



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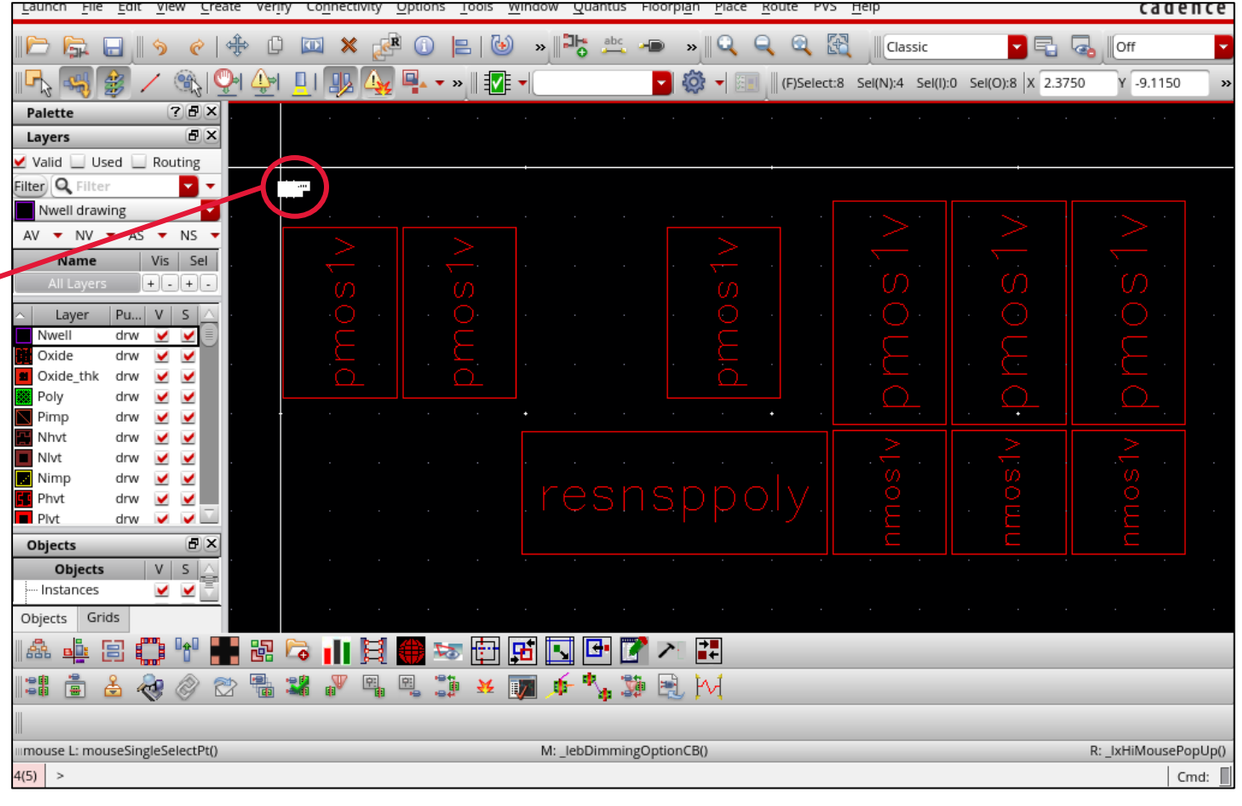
3. Generating the Components *(continued)*

- Below is a zoomed in view of the pins. Notice the label on each pin.



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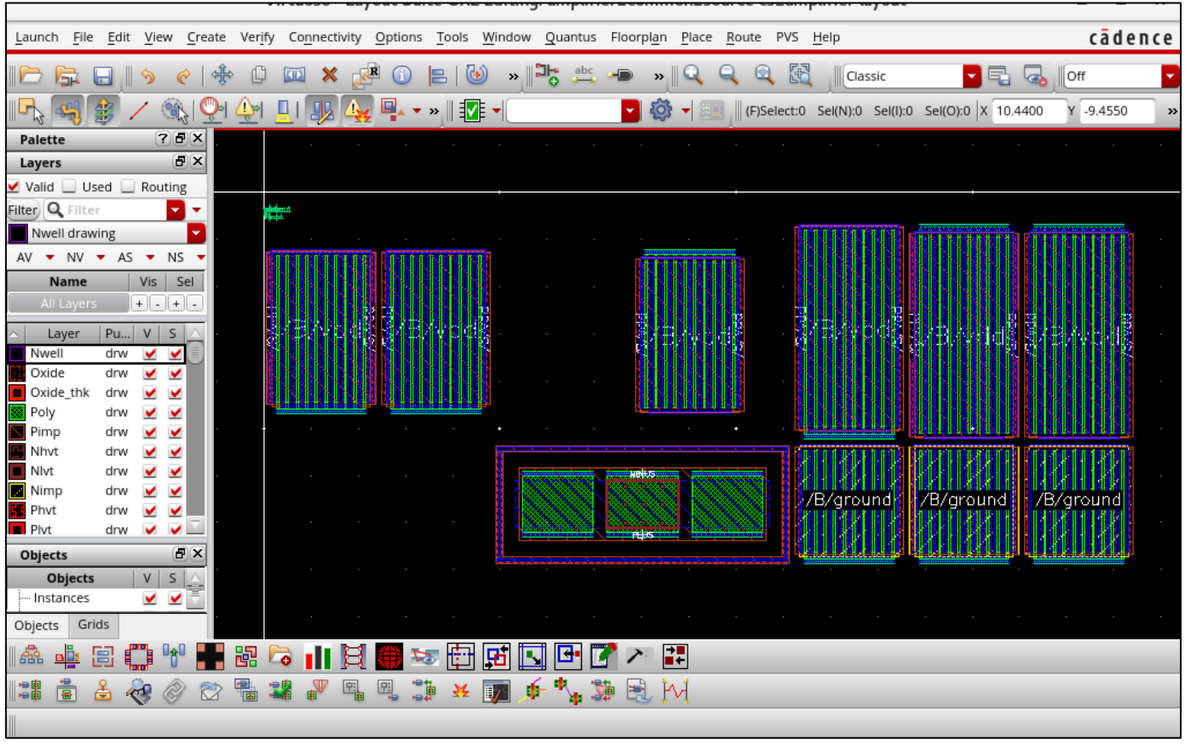
- Adding Dummy Transistors
- Layout MXL Overview
- **Generating the Components**
- Placing the Components
- Routing the Components

3. Generating the Components *(continued)*

- Press **Shift + F** to view the terminals of each transistor.
- Zoom in and out using **Ctrl + Z** and **Shift + Z** respectively (or the scroll-wheel), to see the terminals of each transistor.



- The parameters have affected the dimensions of the transistor, and the number of fingers showed us the multiple drain, gate, and source of each MOSFET.
- Notice how the tool generated the connection between all drains, gates, and sources.
- Press **CTRL + F** to hide the terminals

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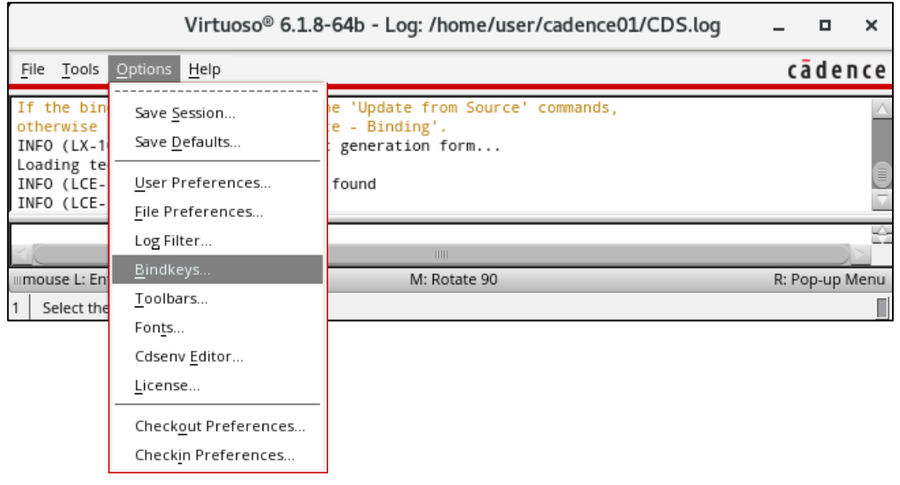
3. Generating the Components *(continued)*

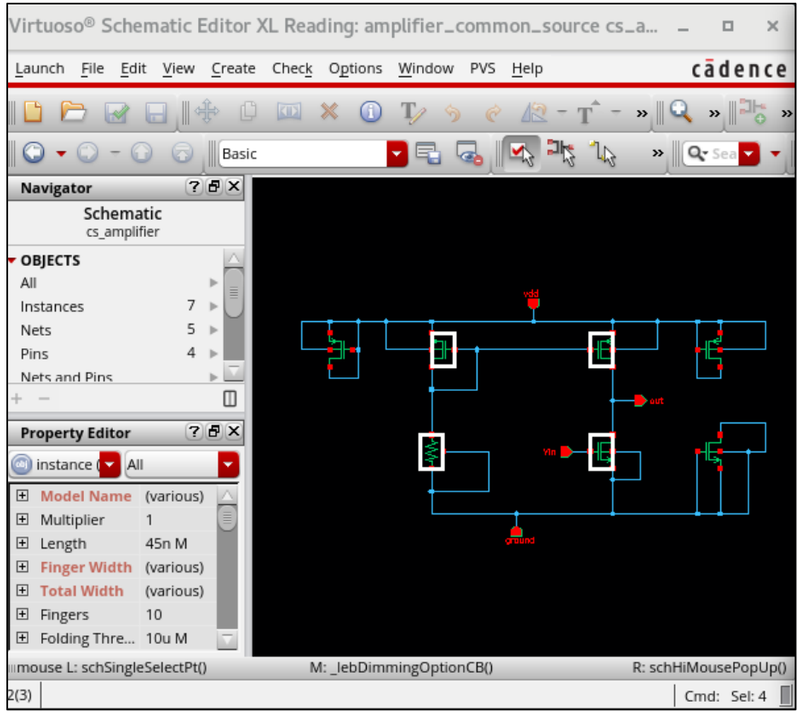
- In order to make things easier, some useful keybinds are mentioned below:
  - To move any object: **M**
  - To draw a rectangle: **R**
  - To create a path: **P**
  - To stretch a path: **S**
  - To create a ruler: **K**
  - To delete all rulers: **Shift + K**
- To get the full list of the keybinds, from the CIW → Options → Bindkeys, and select Layout.

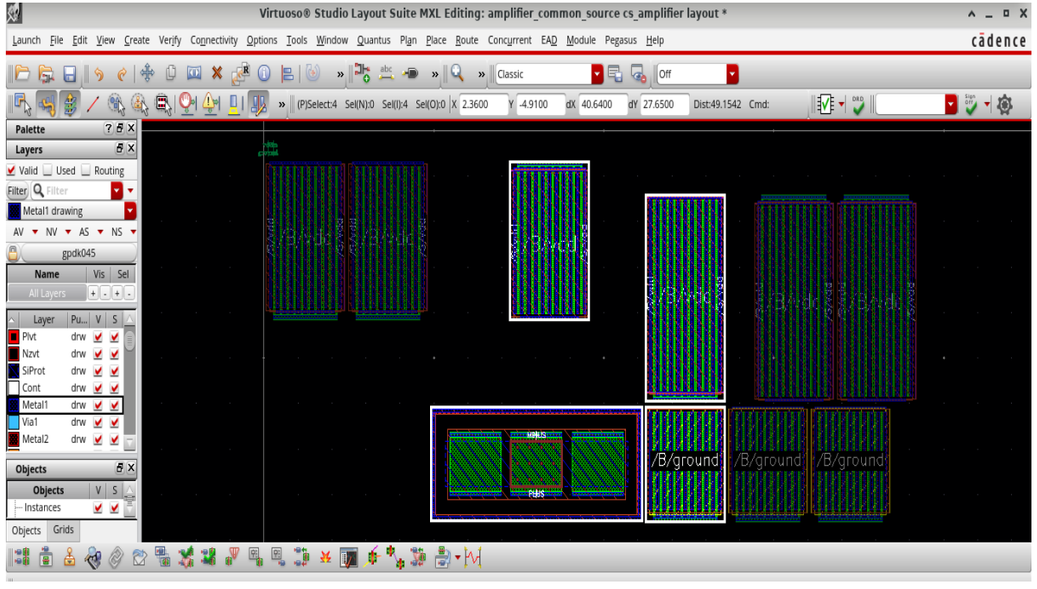


4. Placing the Components

4. Placing the Components

- It is recommended to have the schematic opened next to the layout.
- When a component is selected in the schematic, it will be highlighted in the layout (the opposite is true).





- If the terminals are not generated, select the transistor in the layout view and from the Parameter tab, change the Gate and S/D connection as mentioned in slides 8, 9, 10 and 11 for the dummy devices, and for the actual devices check **Module 2 slide 63 and 64**.

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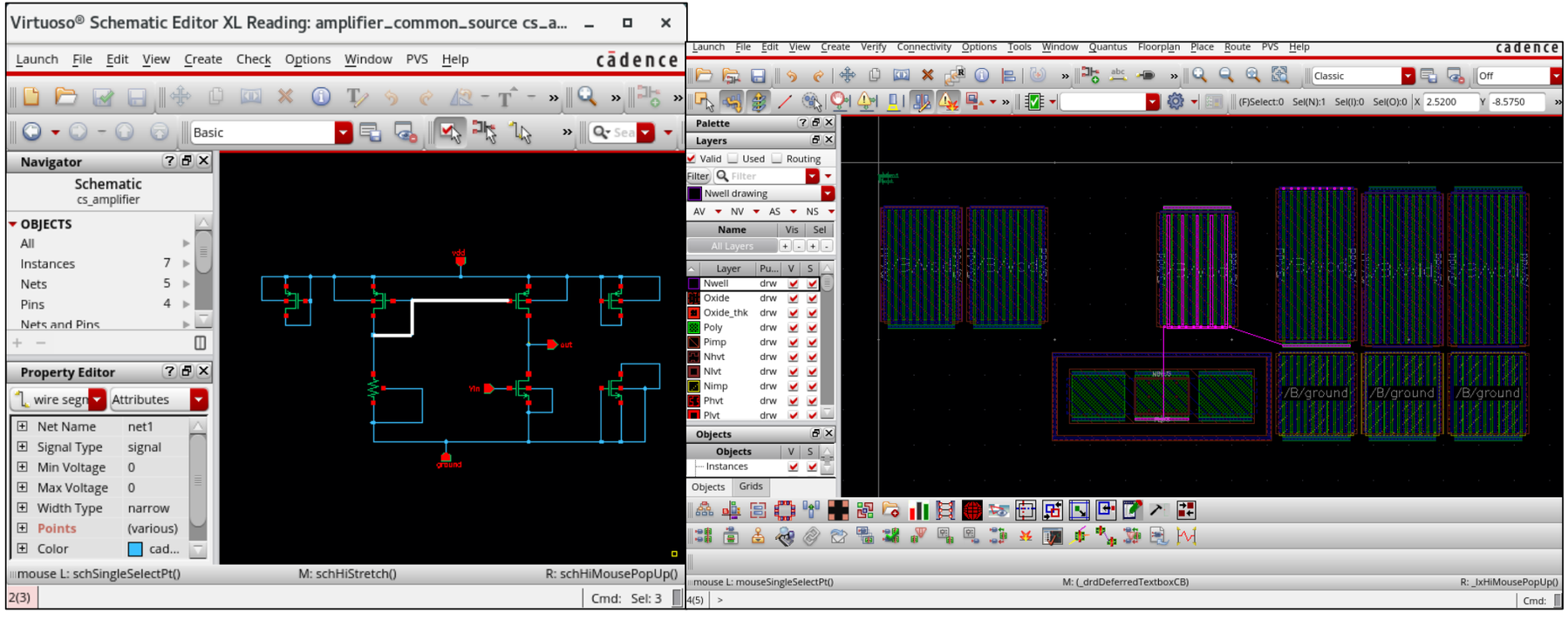
4. Placing the Components *(continued)*

- Similarly, when a net is selected in the schematic, it will be highlighted in the layout as shown below.



- Schematic-driven layout feature, is available in Virtuoso Layout MXL. It highlights where to connect each component in the layout view.

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- Adding Dummy Transistors
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- **Placing the Components**
- Routing the Components

4. Placing the Components *(continued)*

- In order to move any devices in any angle around the canvas, click on the icon (from the toolbar)  once to make it as such  ().
- Always select the transistor in the schematic to know which one it is in the layout.
- Select the NMOS from the schematic. It is now selected in the layout. From the Layout MXL, select Edit → Move (or press “M” on the keyboard) and move it downwards (shown next slide).
- Select the resistor, press M and place it above the NMOS.
- To create a Ruler, press K on the keyboard, and make sure the distance between the NMOS and the resistor is 1 µm.
- Select the left PMOS from the schematic (the PMOS that is part of the actual design). It is now selected in the layout, press M and place it above the resistor. Make sure the distance between the resistor and the PMOS is 1 µm.
- Select the right PMOS from the schematic (the PMOS that is part of the actual design). It is now selected in the layout, press M and place it above the PMOS. Make sure the distance between the two PMOS transistors is 0.5 µm.

- Note that you can zoom in and out using your mouse wheel. Also, you can click and hold on your middle mouse button to move around the canvas.

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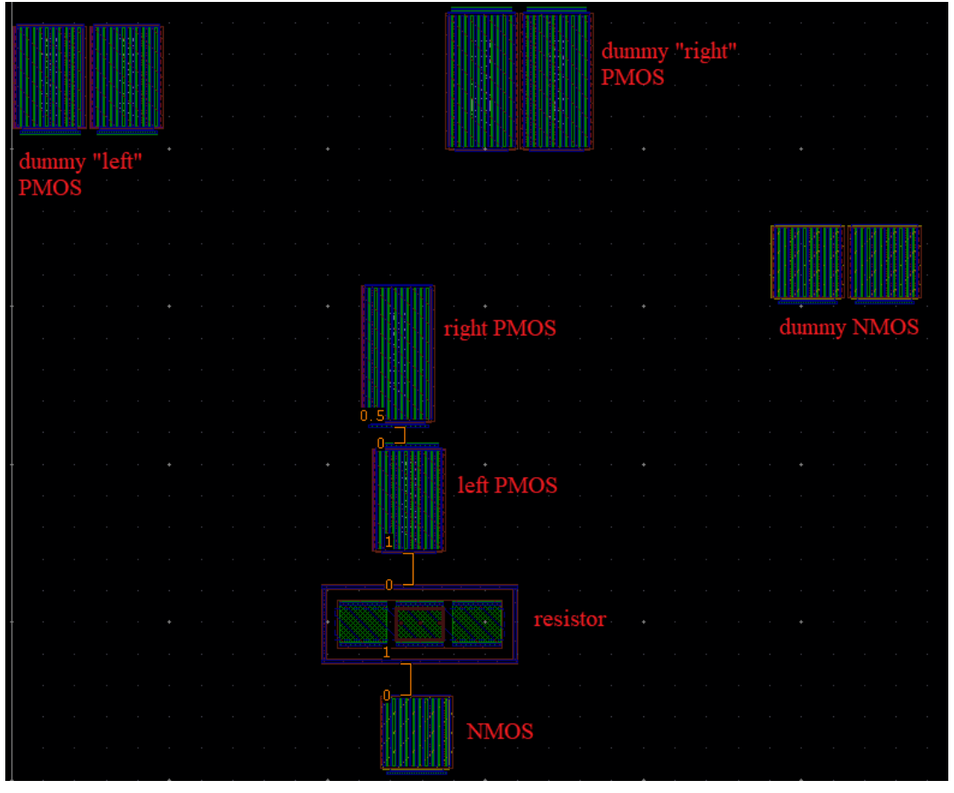
4. Placing the Components *(continued)*

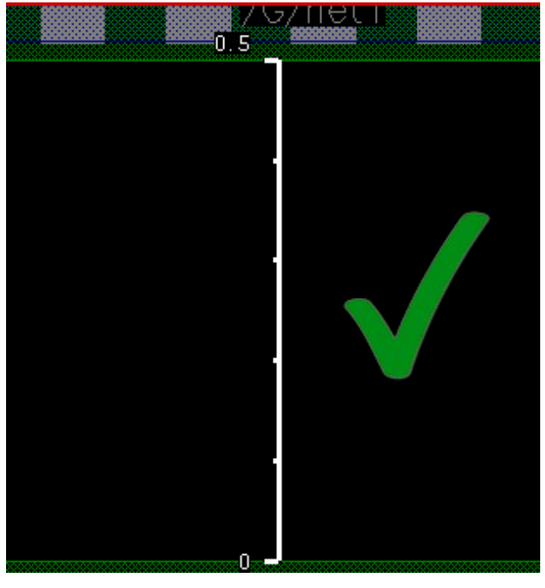
- The steps that were mentioned in the previous slide are shown in the figure below.
- The rest of the transistors are the dummy transistors. We will place each dummy transistor on both sides of the actual corresponding transistor.

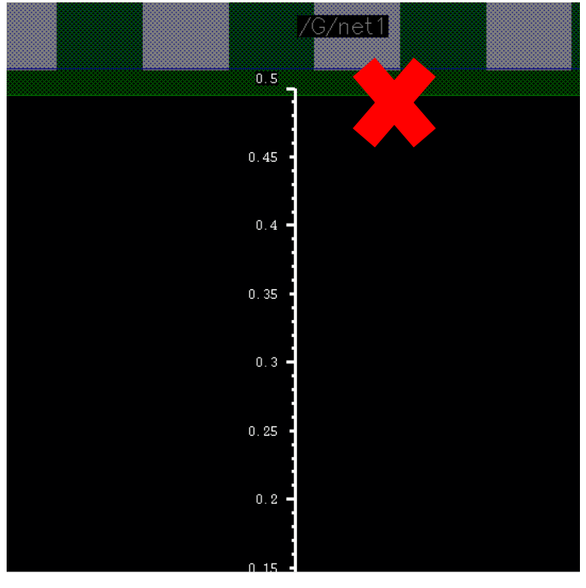


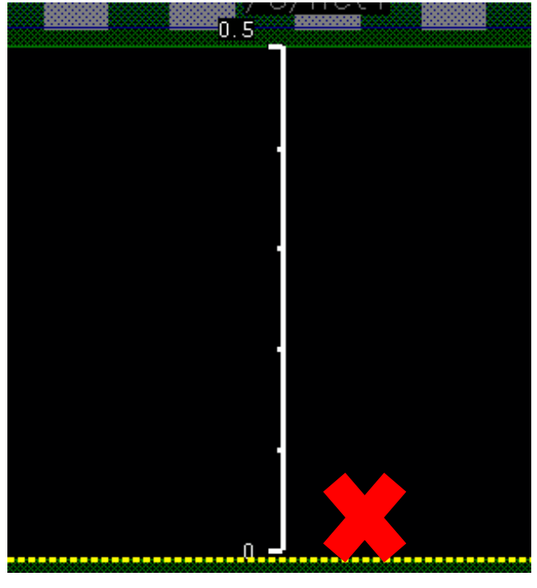
- Note that you can select each dummy transistor in the schematic to make sure which one it is in the layout.
- Another quick tip is to press F to zoom in an absolute scale the current window

4. Placing the Components *(continued)*

- The measurements must be precisely as indicated because this is very critical.
- Make sure you use the ruler correctly, and take extremely small, precise measurements.



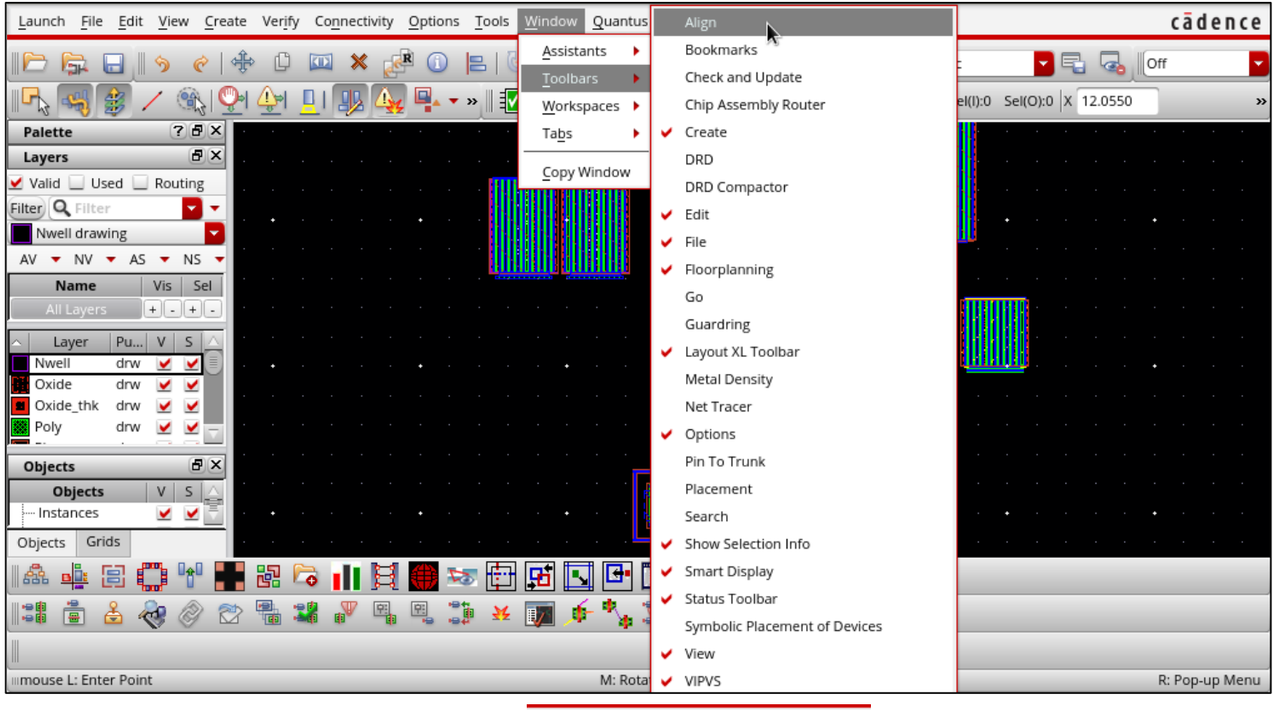




- Make sure that the tip of the ruler is always exactly on the edge of any component when measuring the distance.

4. Placing the Components *(continued)*

- Notice that the right PMOS, left PMOS, resistor, and the NMOS are not vertically aligned. We must align them vertically because it will ease the routing (i.e., the wiring).
- In order to Align the mentioned transistors vertically, from the toolbar select Window → Toolbars → Align.



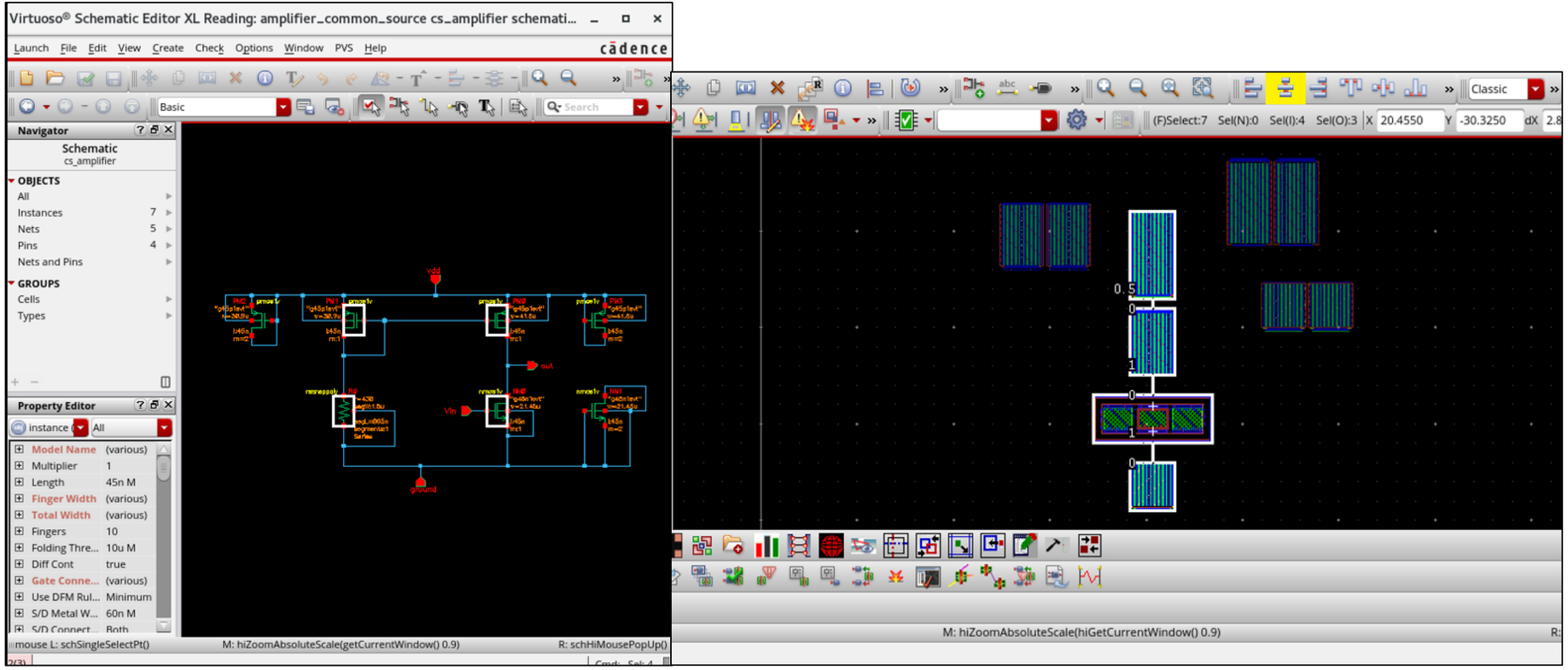
- The following icons will be added in the toolbar  .

AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

4. Placing the Components *(continued)*

- Select the right PMOS, left PMOS, resistor, and the NMOS and select the icon  to align them vertically.



- Note that this step is important because later when we wire the transistors, the connection must be in contact with the other transistor.

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AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- **Placing the Components**
- Routing the Components

4. Placing the Components *(continued)*

- The next steps involve placing the corresponding dummy transistors on the sides of the actual transistor.
- Select the NMOS dummy transistor from the schematic to highlight it in the layout.
- Since the Multiplier of the dummy device was set to 2, we have two NMOS dummy transistors in the layout and they will be placed on each side of the NMOS.
- Place one of the dummy NMOS transistors on one side of the NMOS, and the other dummy NMOS transistor on the other side.
- Make sure to have a minimum distance of 0.12 µm between the NMOS and the dummy NMOS transistor (Minimum N+ Implant space is 0.12 µm, i.e., between two Nimp layers).
- Also, make sure not to move the NMOS transistor that is part of the design, since it must be aligned vertically with the other devices that are part of the actual design.
- Similarly, select the “left” PMOS dummy transistor from the schematic to highlight it in the layout. Place one of the dummy transistors on one side of the PMOS, and the other dummy PMOS transistor on the other side.
- Make sure to have a minimum distance of 0.12 µm between the PMOS and the dummy PMOS transistors (Minimum P+ Implant space is 0.12 µm, i.e., between two Pimp layers).

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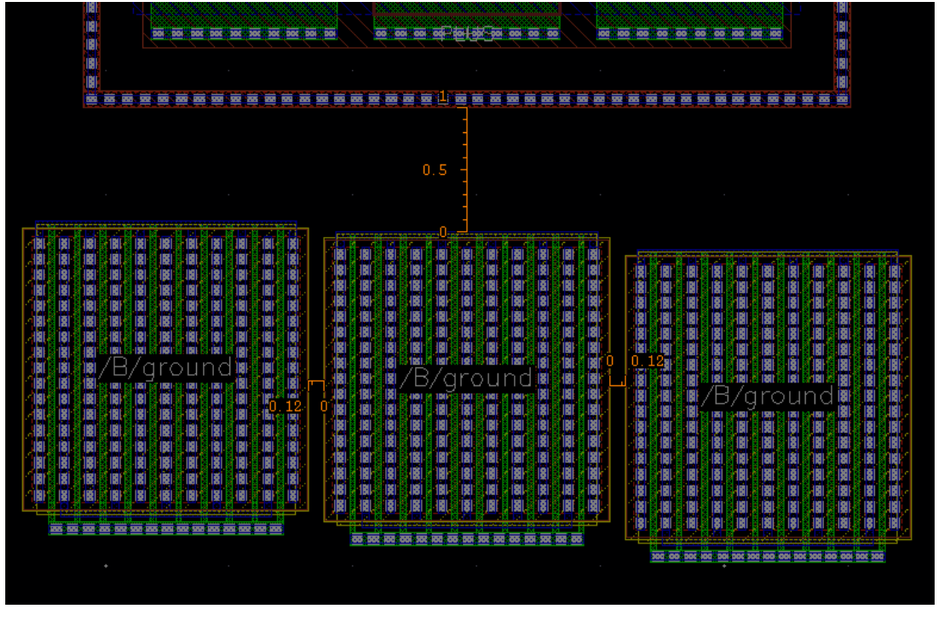
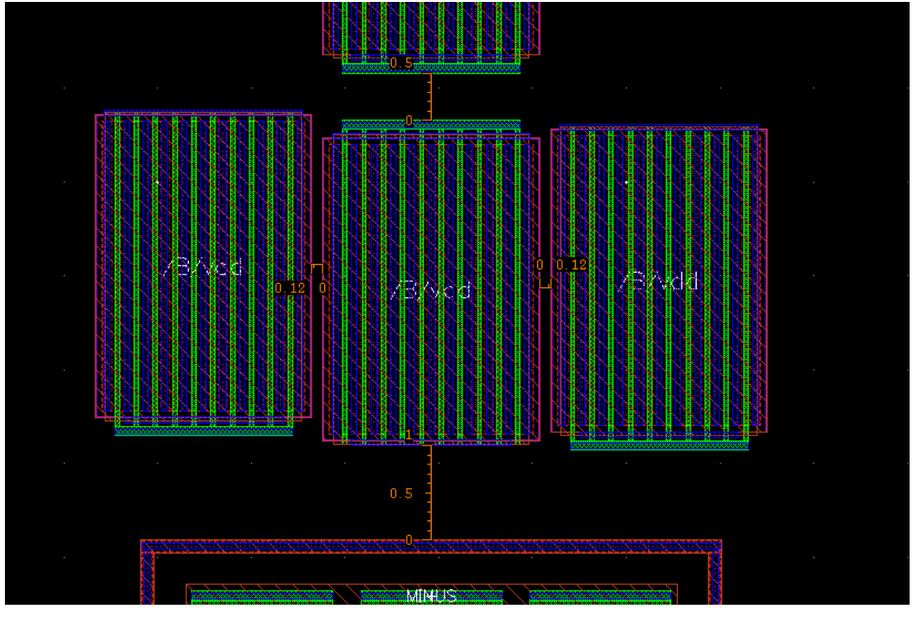
AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- **Placing the Components**
- Routing the Components

4. Placing the Components *(continued)*

- Make sure not to move the resistor and the transistors that are part of the actual design.
- The steps that were mentioned in the previous slide are shown in the figures below.
- Notice that the transistors are not horizontally aligned.
- Select the NMOS transistors, from the toolbar click on the icon  to align horizontally.
- Similarly, align the PMOS transistors horizontally.
- Make sure the distance between the resistor and the PMOS remains 1 µm.





- Minimum distance between two Nimp layers (yellow layer of the NMOS transistor) is 0.12 µm.
- Minimum distance between two Pimp layers (red layer of the PMOS transistor) is 0.12 µm.
- It is possible to select multiple transistors by holding the key Shift and left clicking

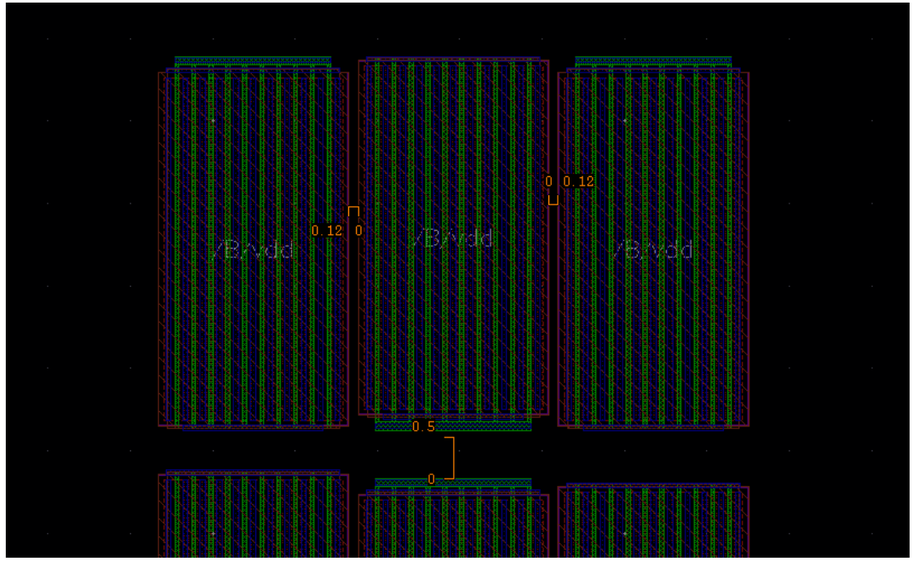
cadence

AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- **Placing the Components**
- Routing the Components

4. Placing the Components *(continued)*

- Similarly, select the “right” PMOS dummy transistor from the schematic to highlight it in the layout. Place one of the dummy transistors on one side of the PMOS, and the other dummy PMOS transistor on the other side.
- Make sure to have a minimum distance of 0.12 µm between the PMOS and the dummy PMOS transistor (minimum spacing between two Pimp layers).
- After placing the dummy transistors, select the three PMOS transistors and align them horizontally.
- Make sure to keep the distance 0.5 µm vertically between the two PMOS transistors.



- Make sure not to move the resistor and the transistors that are part of the actual design. To get a minimum distance of 0.12 µm, move the dummy devices closer to the PMOS transistor.

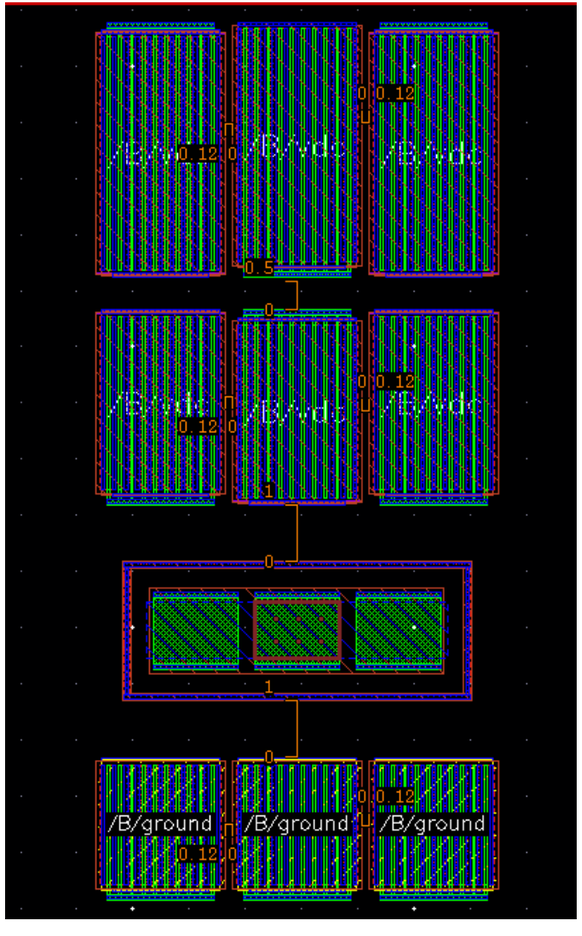
cadence

AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- **Placing the Components**
- Routing the Components

4. Placing the Components *(continued)*

- The figure below combines all the previous work.



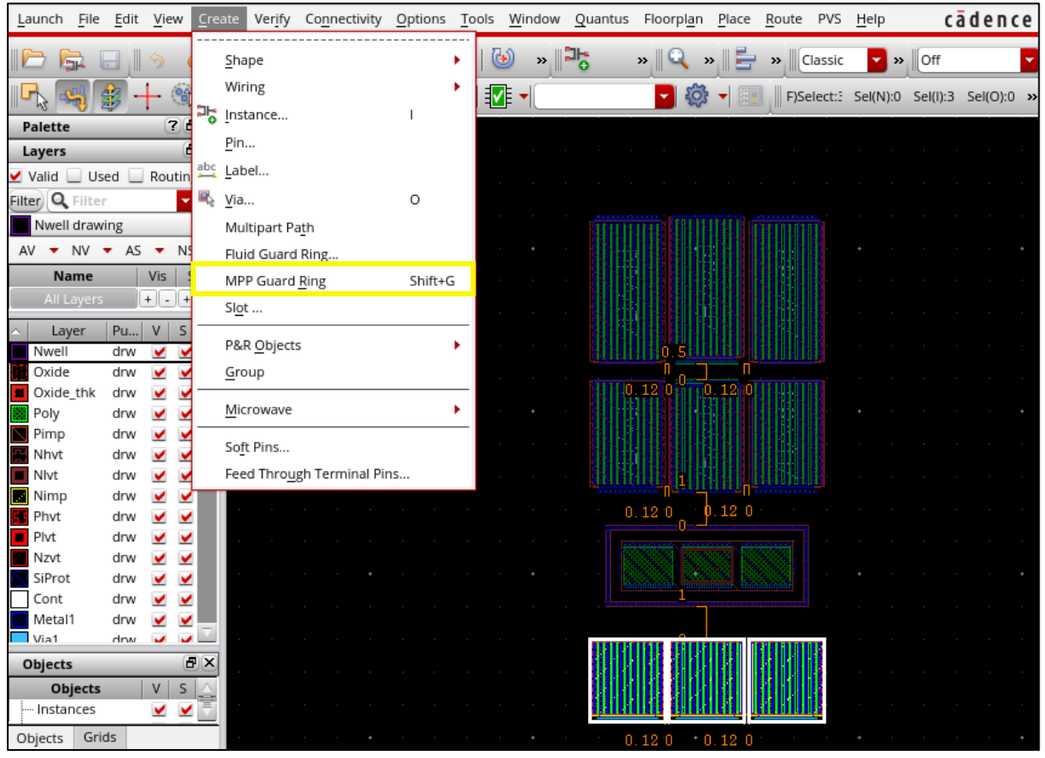
- Our goal is to optimize the layout, meaning to reduce the parasitic (RC) effects.
- We reduce the area by placing the components close to each other as much as possible. This will also reduce the parasitic effects.

cadence

5. Routing the Components

5. Routing the Components

- We will now start drawing the bulk of the transistors.
- The bulk of the NMOS transistor is made of P-Tap. We will use what is called a Guard Ring to surround the transistors automatically.
- Select the three NMOS transistors. From the toolbar choose Create → MMP Guard Ring (or Shift + G).



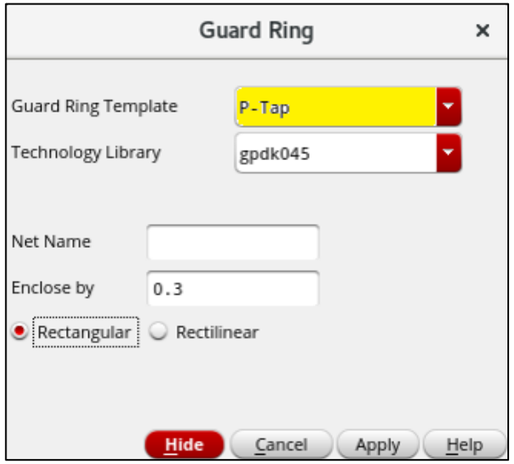
- The body or the bulk, is the 4th terminal of a transistor. It has to be created manually in the layout since we selected the bodytie type to be **none** in Module 2.

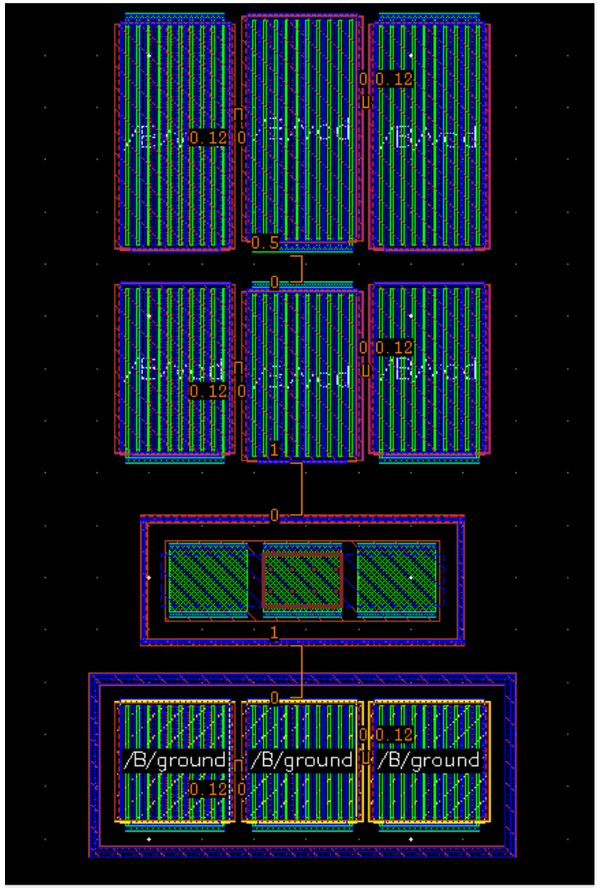
AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

5. Routing the Components *(continued)*

- The Guard Ring form pops-up.
- From the drop-down list of the Guard Ring Template, select **P-Tap**.
- Enclose by 0.3 and select Rectangular.
- Click Apply and close the form.
- Notice how the bulk is drawn around the NMOS transistors.





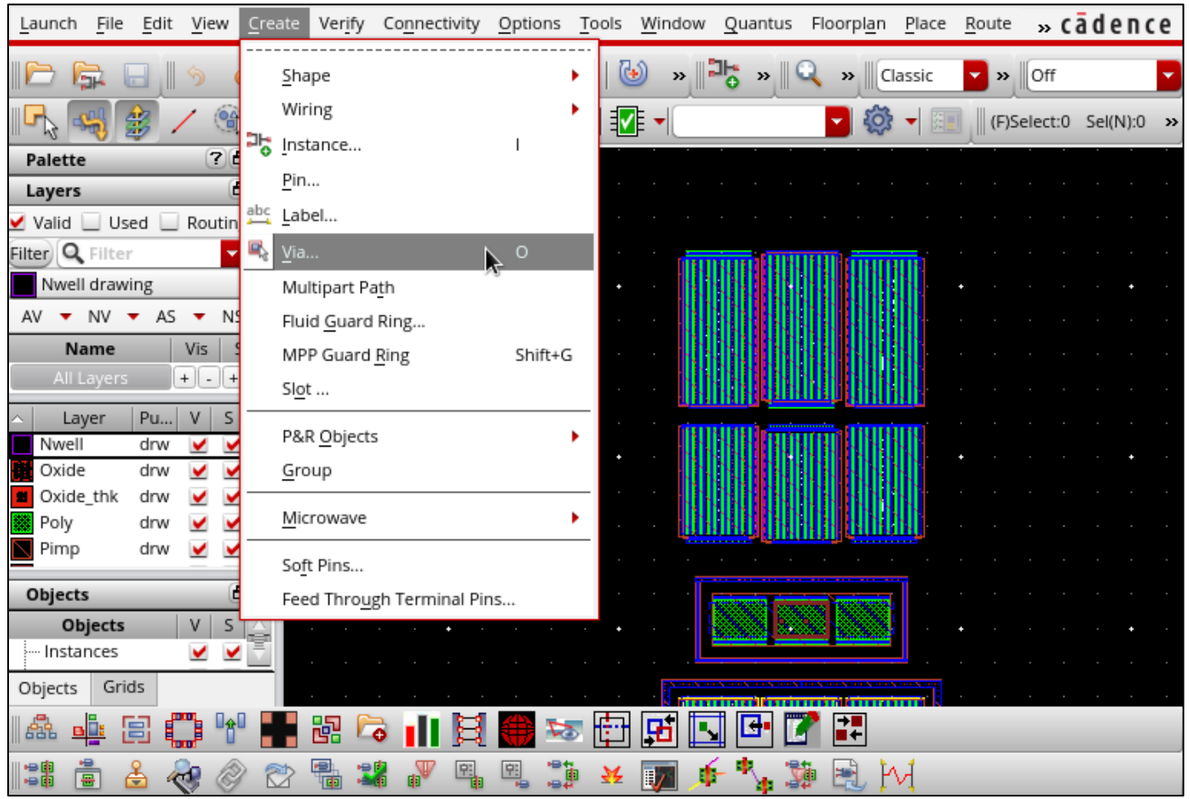
cadence

AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

5. Routing the Components *(continued)*

- Since the bulk of the NMOS transistors are connected to ground, we must connect the pin “ground” to the bulk.
- Because the pin is of type metal3, we must first establish a via stack on the bulk of the transistor from metal1 to metal3, then draw a metal route to the outside, and finally position the pin ground on it.
- To create a via, from the toolbar choose Create → Via… (or press O).

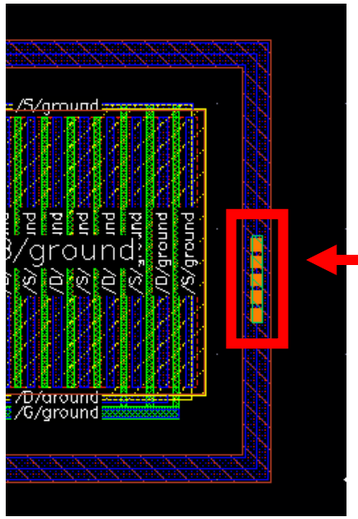


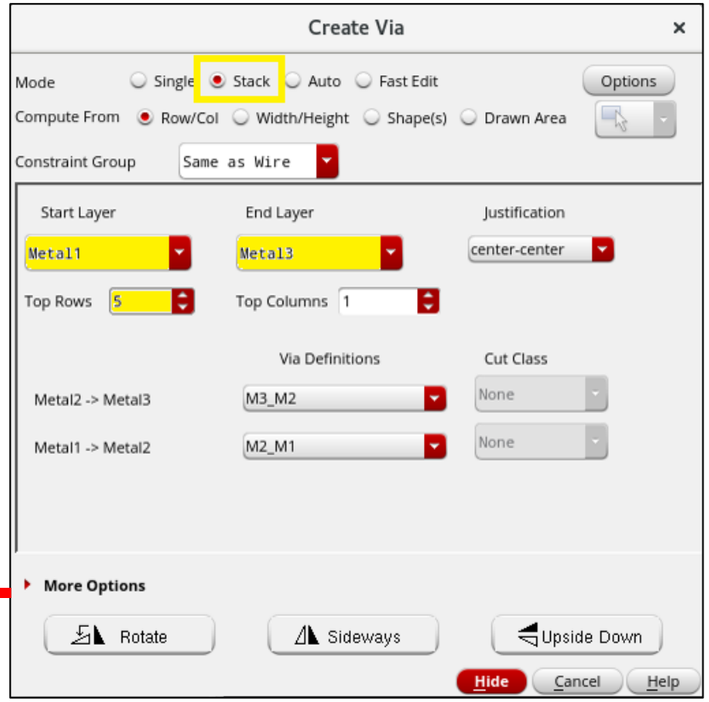
- Check slide 27 if you cannot find the pins. When highlighted it looks like a dot since it is small with respect to the other devices.

cadence

5. Routing the Components *(continued)*

- The “create via” option will pop up. Make sure to first select the **stack** option.
- Change the Start Layer to **Metal1** and the End Layer to **Metal3**.
- Change the number of rows to 5, click on **Hide,** and place the via on the right side of the bulk like shown in the picture below**.**

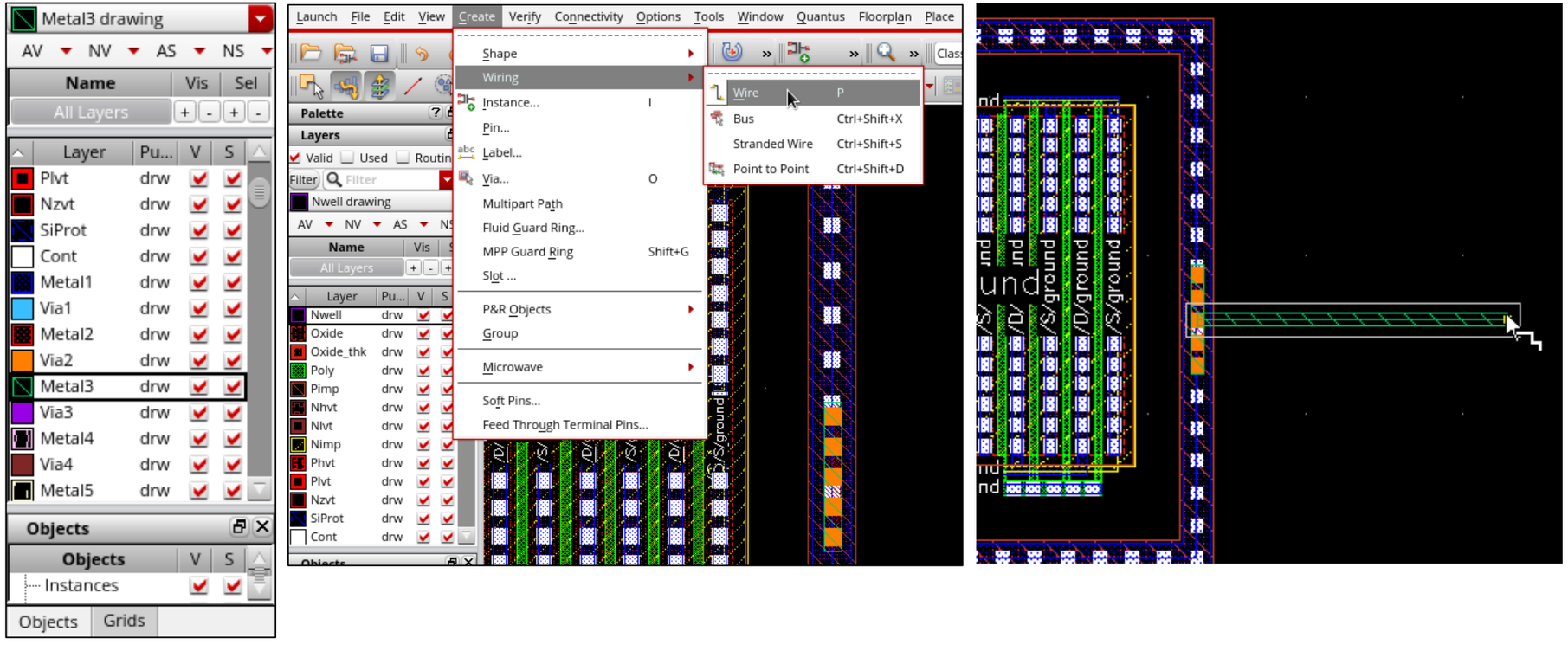




cadence

5. Routing the Components *(continued)*

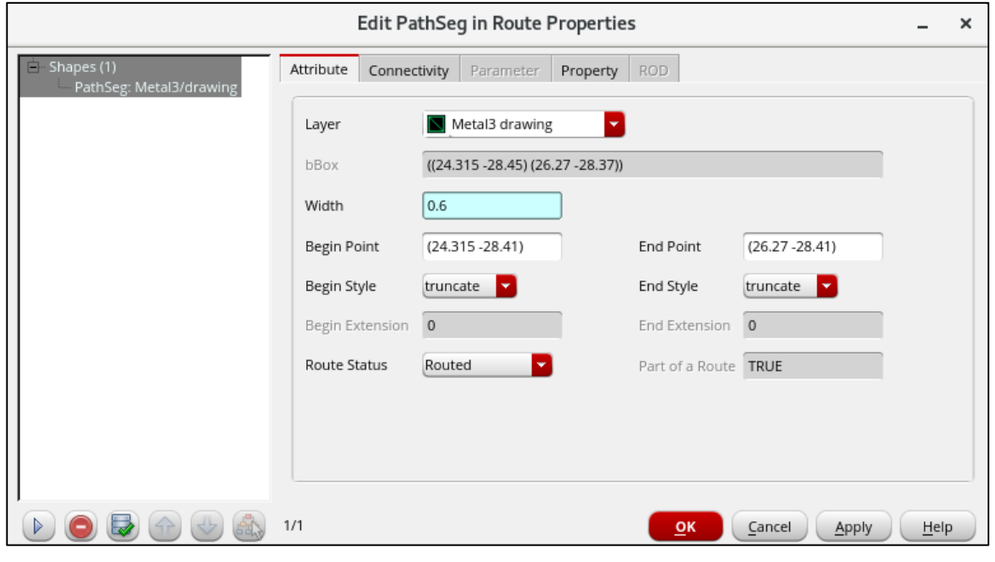
- The next step is to create a path using Metal3, to place the pin and label on it. First select Metal3 drawing from the Layer Selection Window (LSW).
- From the toolbar choose Create → Wiring → Wires, or Press P.

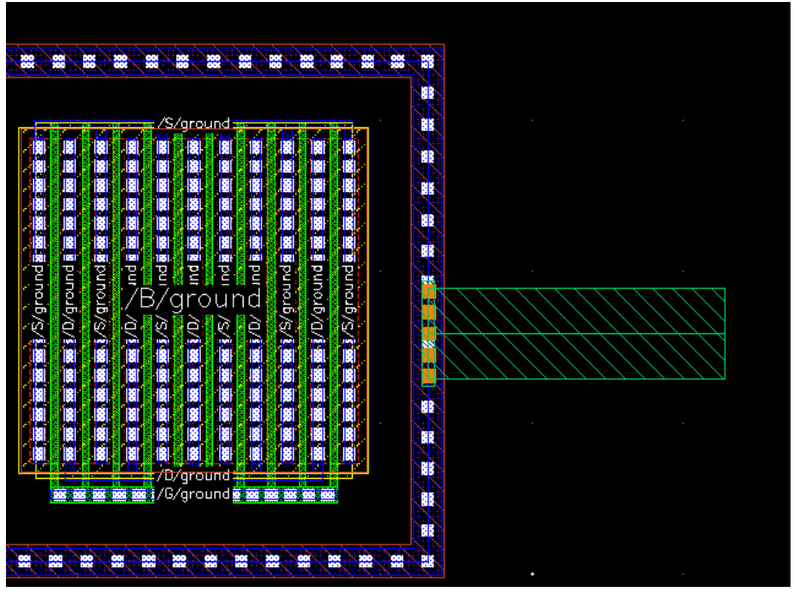


- Keep in mind that all you need to do to draw a pass is to click once on your mouse's right click and drag it to the desired location. Once you're done, hit the enter bindkey.

5. Routing the Components *(continued)*

- Select your metal3 path and open its properties by pressing Q.
- Change the Width of the path to 0.6 and click **OK**.
- The result should look like the picture below.

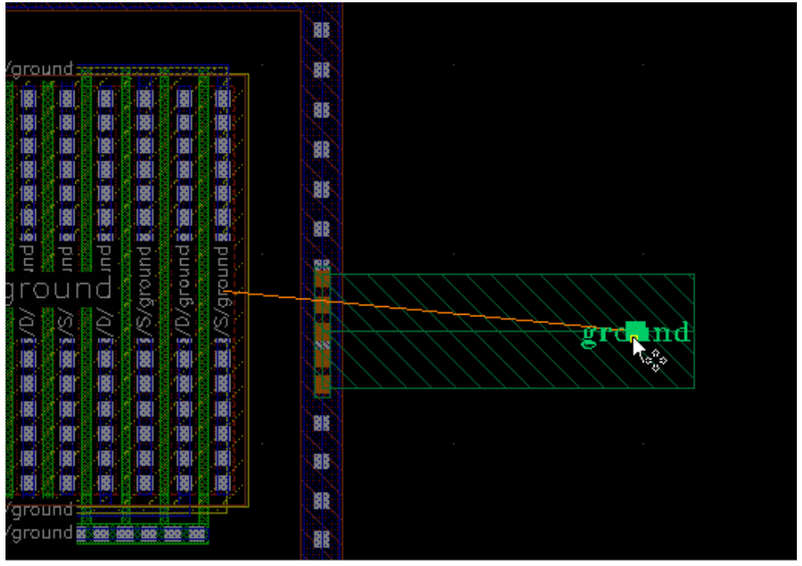




cadence

5. Routing the Components *(continued)*

- Last step is to add the ground pin and its label on top of the path.
- From the schematic, click on the pin ground. It is now highlighted in the layout. Select both the **pin** and the **label** (you can use Shift on the keyboard to select multiple objects), and press M to move and place it on the path that we just placed (if you previously closed the Layout MXL, check slide 18 on how to enable the labels).
- Notice after placing the pin and the label on the bulk, the connection is named “ground”.



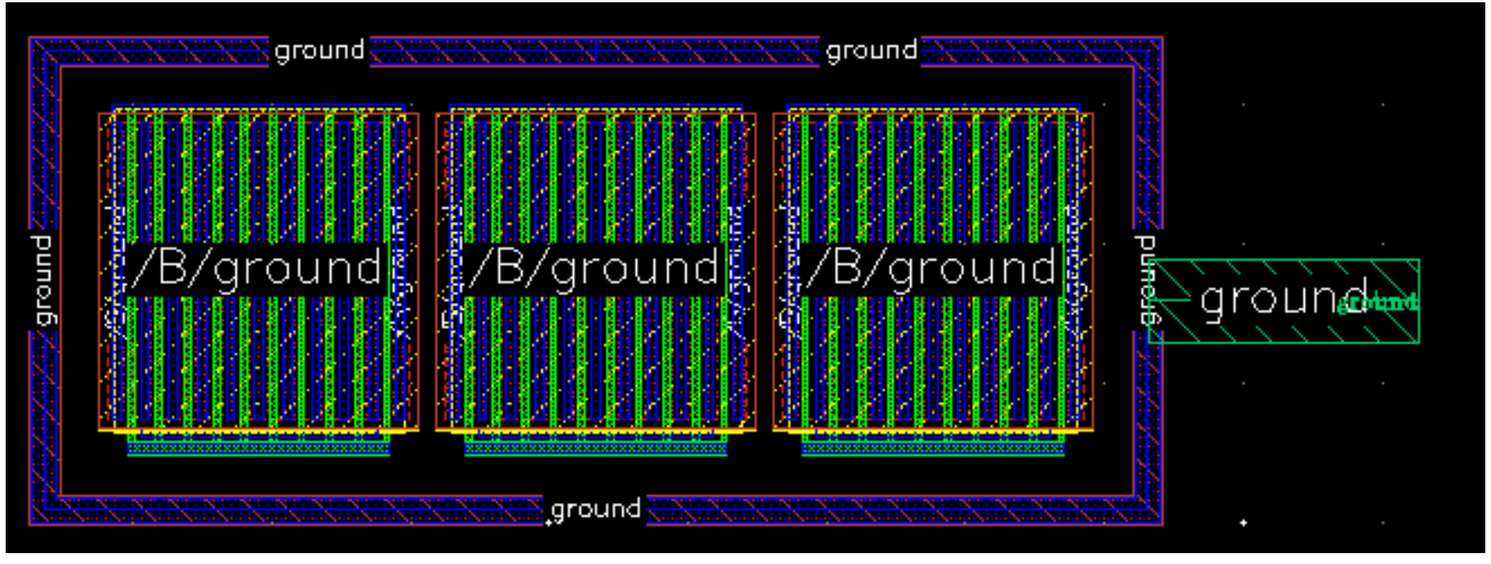
cadence

AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

5. Routing the Components *(continued)*

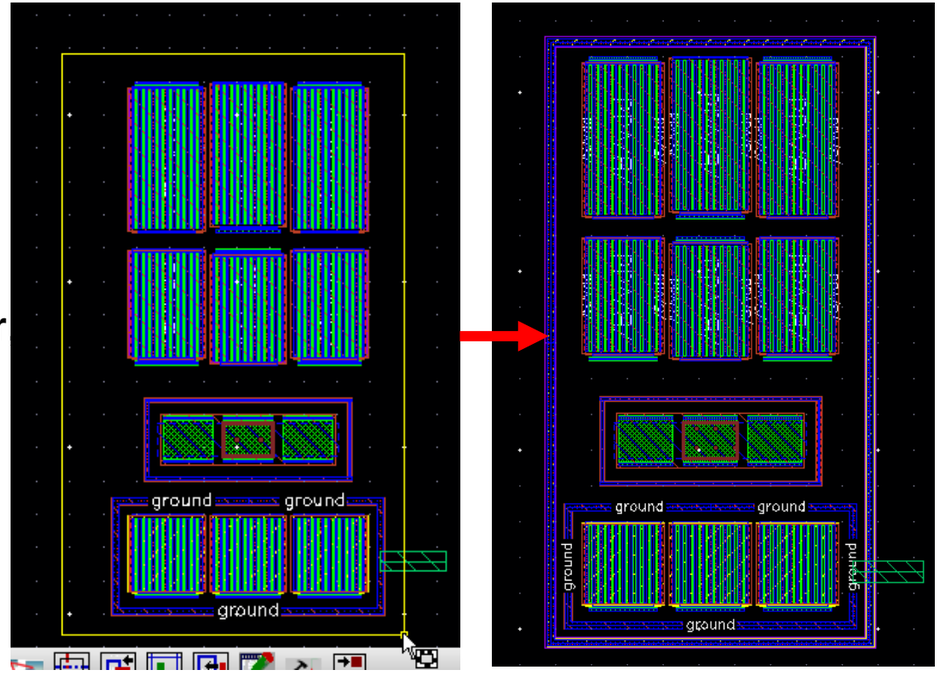
- Notice after placing the pin and the label on the path, the bulk and the connection are named “ground”.



cadence

5. Routing the Components *(continued)*

- The bulk of the PMOS transistor is made of N-Tap.
- Select **all** the devices (including the bulk of the NMOS and excluding the path created earlier) and create a Guard Ring (Shift + G) of **N-Tap** Guard Ring Template.
- Enclose it by 0.3, select the option **rectangular** click Apply, and close the form.
- The figure shows the bulk of the PMOS transistor which also encloses the bulk of the NMOS transistors.

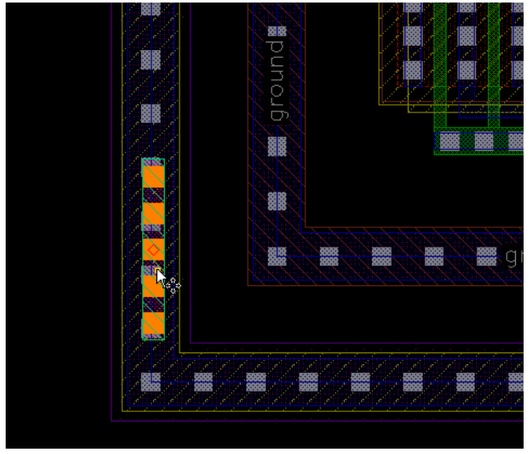


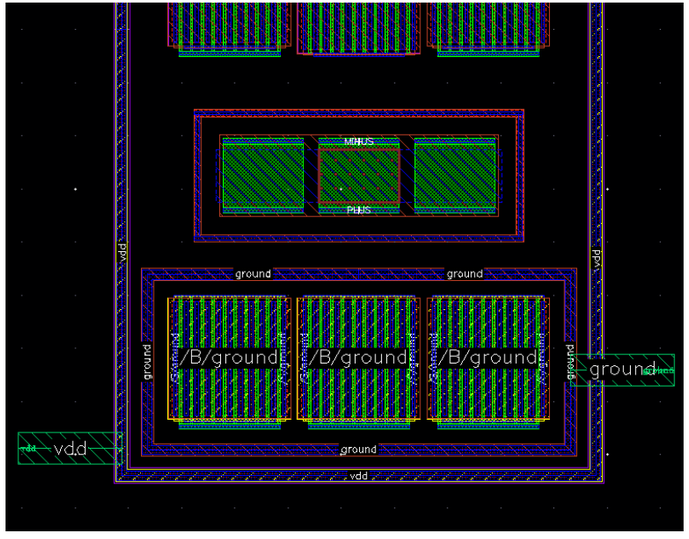
- We want our pins to be visible outside the bulk, this is why it is not inside the N-Tap Ring we just placed.

cadence

5. Routing the Components *(continued)*

- We will repeat the same process for the VDD pin.
- You can copy a via by pressing C and clicking on the previously inserted via, or you can press O to construct a new one with the same parameters as before (Check slide 46).
- Place the via on the bottom left side of the N-Tap bulk we just placed and draw a Metal3 path to the outside.
- Change the width to 0.6 and place the VDD pin and label on top of it.

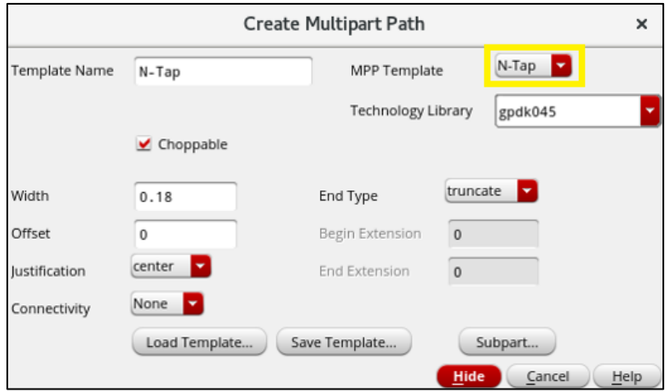




cadence

5. Routing the Components *(continued)*

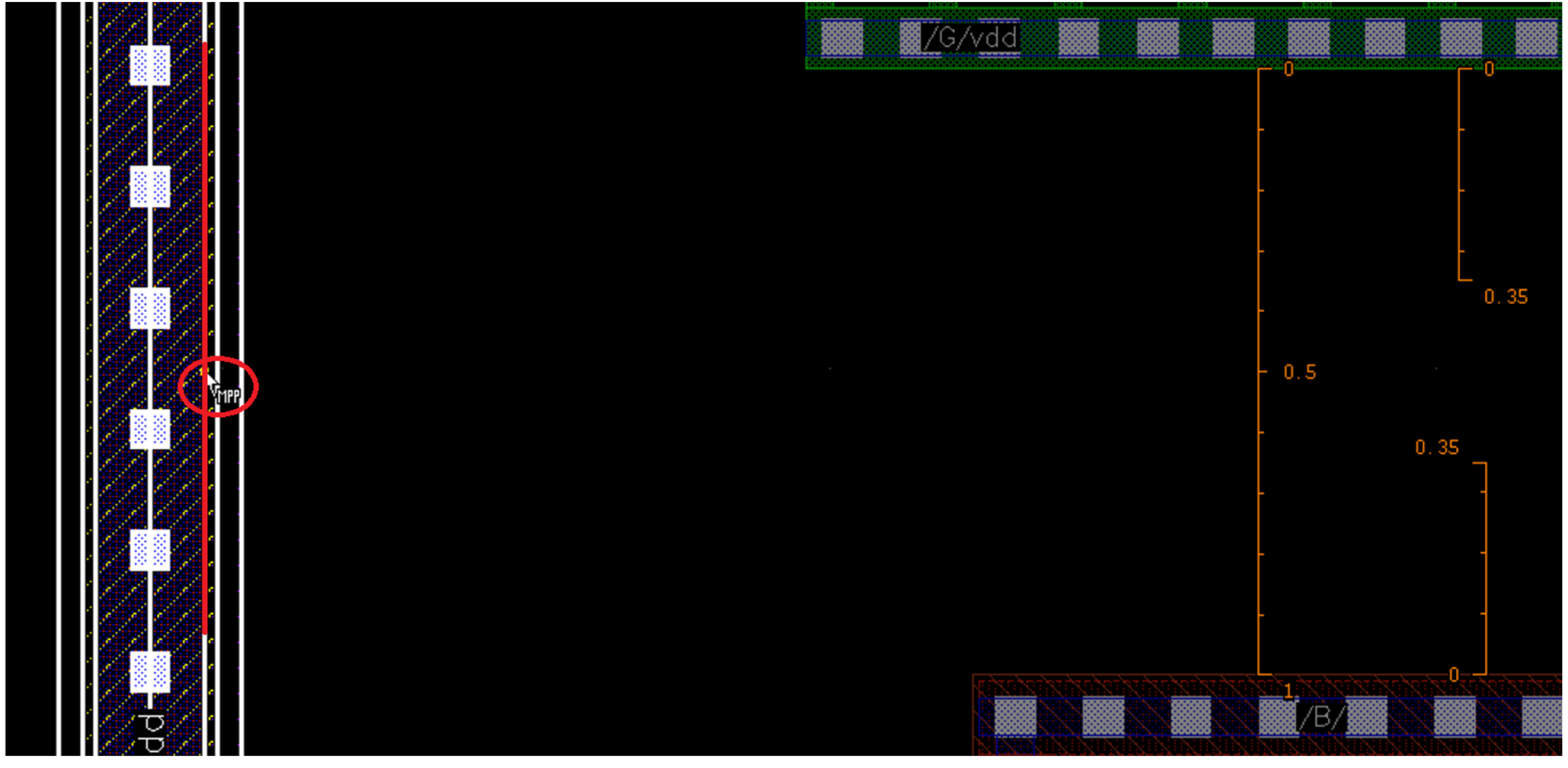
- From the toolbar choose Create → Multipart Path.
- Press F3 on the keyboard (or Fn + F3 in case you have FnLock pressed on your keyboard machine) to open the Create Multipart Path form.
- Select **N-Tap** from the drop-down list of MPP Template and click Hide.



- Make sure the Create/Edit Snap Mode is set to Orthogonal.
- After finishing the Layout, we will run Design Rule Check (DRC) which checks the different dimensions and placement on the canvas (Module 9) and reports any violations.
- In this case, since the path of N-Tap contains the oxide layer, and the guard ring is of the same type, we can place the two oxide layers on top of each other in order not to get any errors later.
- Thus, we need to be careful while placing the path on the next slide.

5. Routing the Components *(continued)*

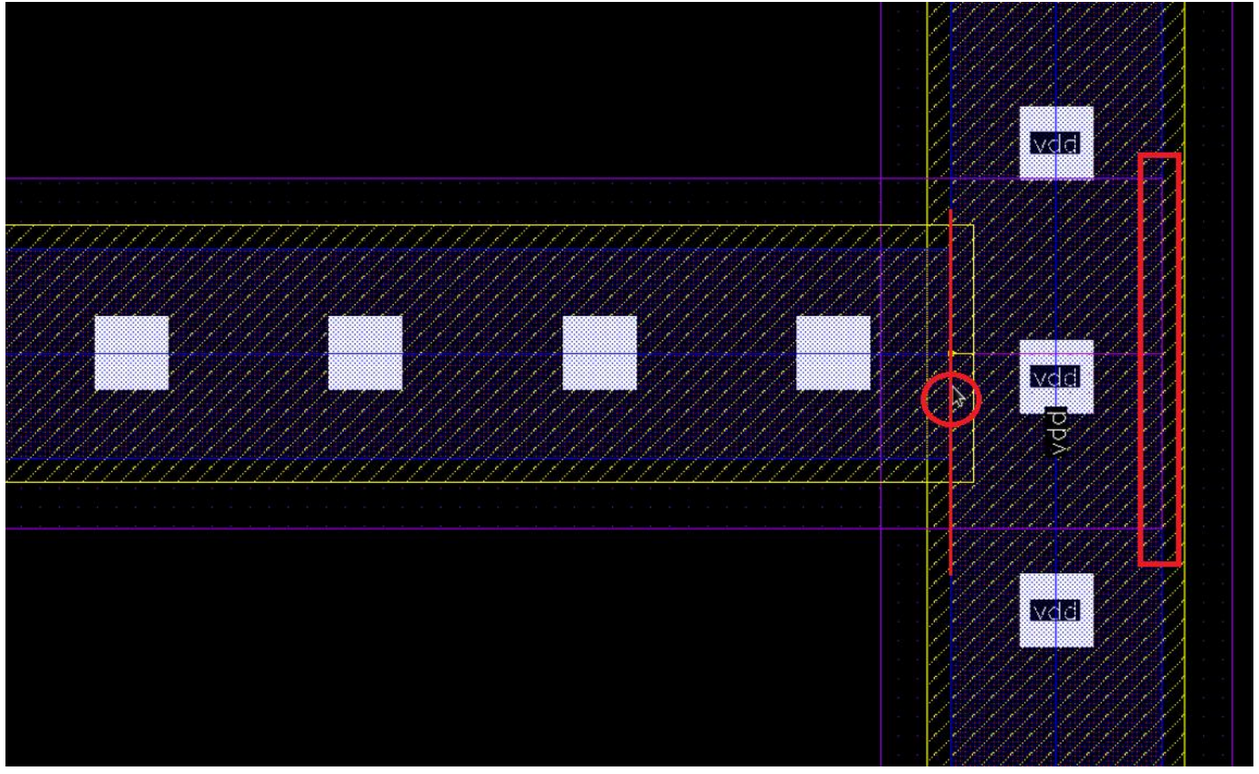
- Place the mouse pointer on the oxide layer as shown below, extend it to the other side, and again place the mouse pointer on the oxide layer (shown next slide) and press enter to confirm the path.



- Keep in mind that it's important to position the pointer precisely where it appears in the image.

5. Routing the Components *(continued)*

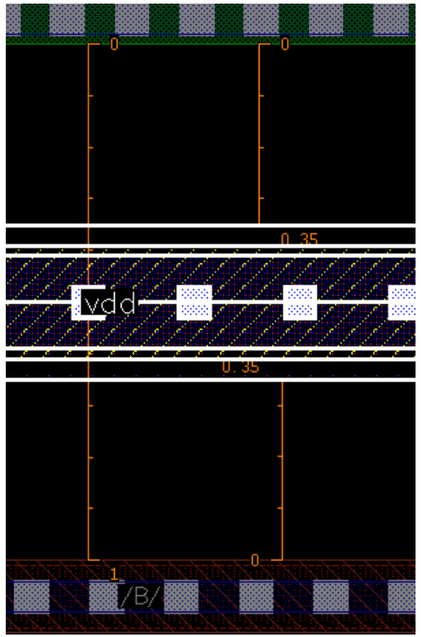
- After extending the path from one side, place the mouse pointer on the oxide layer as shown and press **enter** on the keyboard to confirm the path.

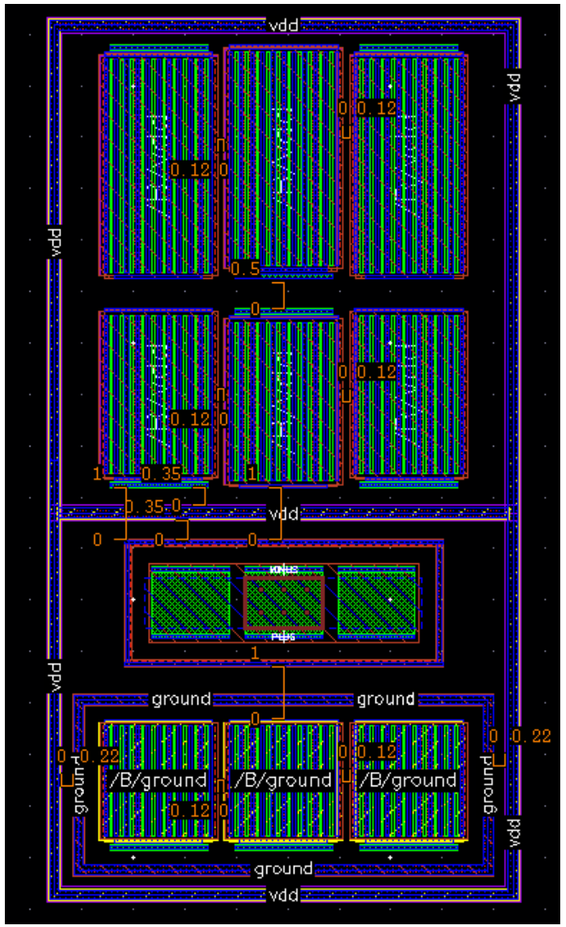


- Note that to confirm the path, do not press on your mouse's right click. Instead press **enter**.
- Note that the path and the oxide layer should match exactly as highlighted in the image

5. Routing the Components *(continued)*

- Press on M and select the path to move it according to the measurements shown in the first picture.
- Your work should be similar.

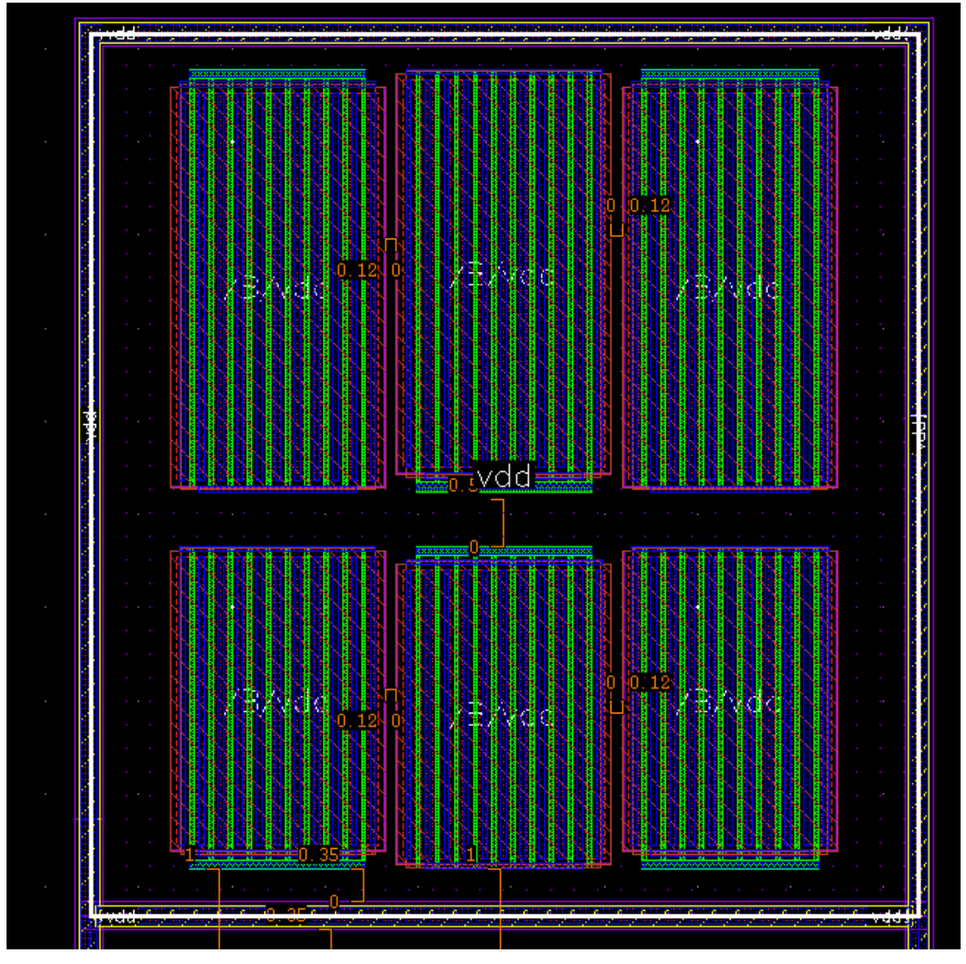


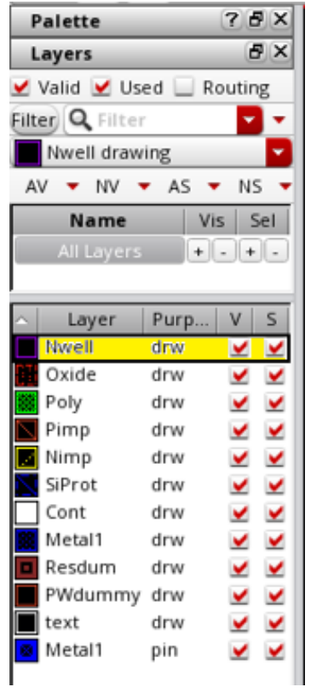


- Note that two rulers were created with length of 0.35 um from each side so that the Multipart path is exactly between the transistor and the resistor.

5. Routing the Components *(continued)*

- Also, we need to add an Nwell layer for the PMOS transistors.
- From Layer Selection Window (LSW), click on used and select the Nwell layer.
- From the toolbar select Create → Shape → Rectangle (or simply press R on the keyboard).
- From one corner of the guard ring, right click to start drawing the rectangle.
- Extend the rectangle diagonally to the other corner. When done the Nwell layer should cover completely the PMOS transistors and half of the guard ring.
- The highlighted rectangle shown in the figure is the drawn Nwell layer.





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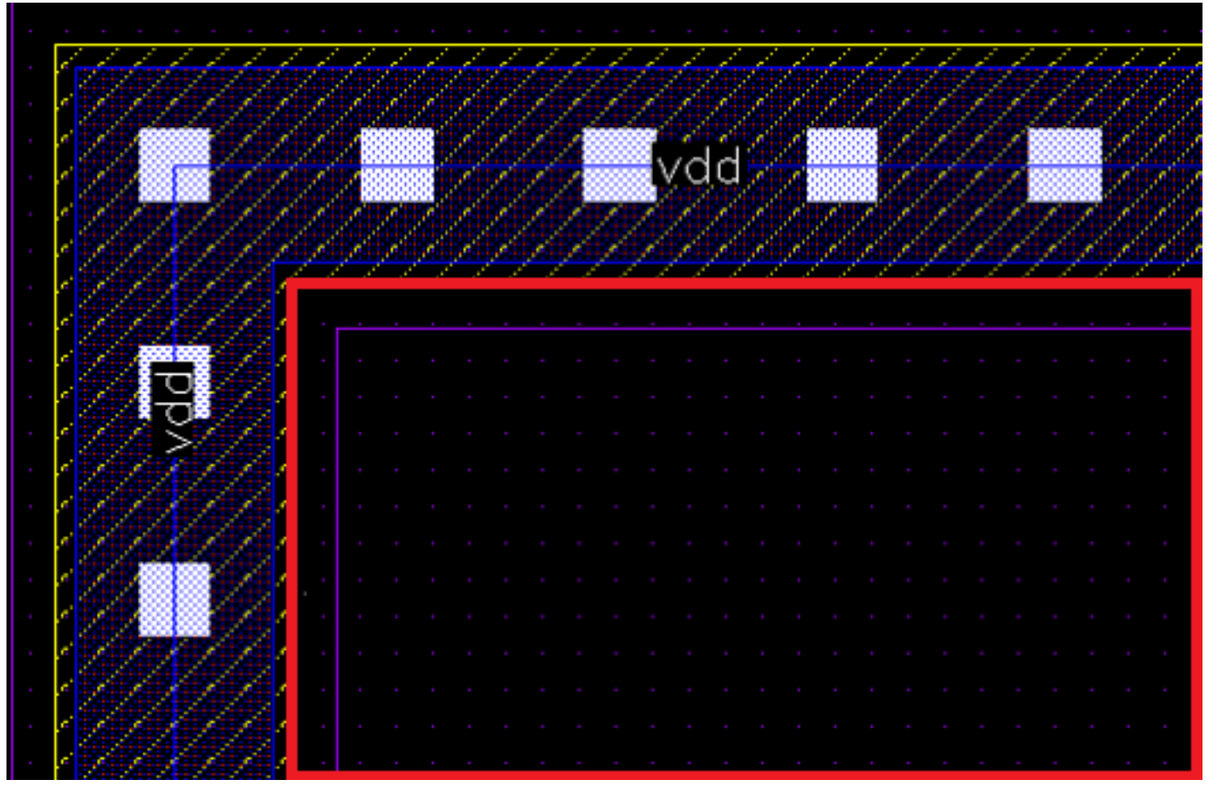
AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

5. Routing the Components *(continued)*

- To make sure that you have placed the N well layer, small purple dots should be visible like shown in the image in the highlighted red box.



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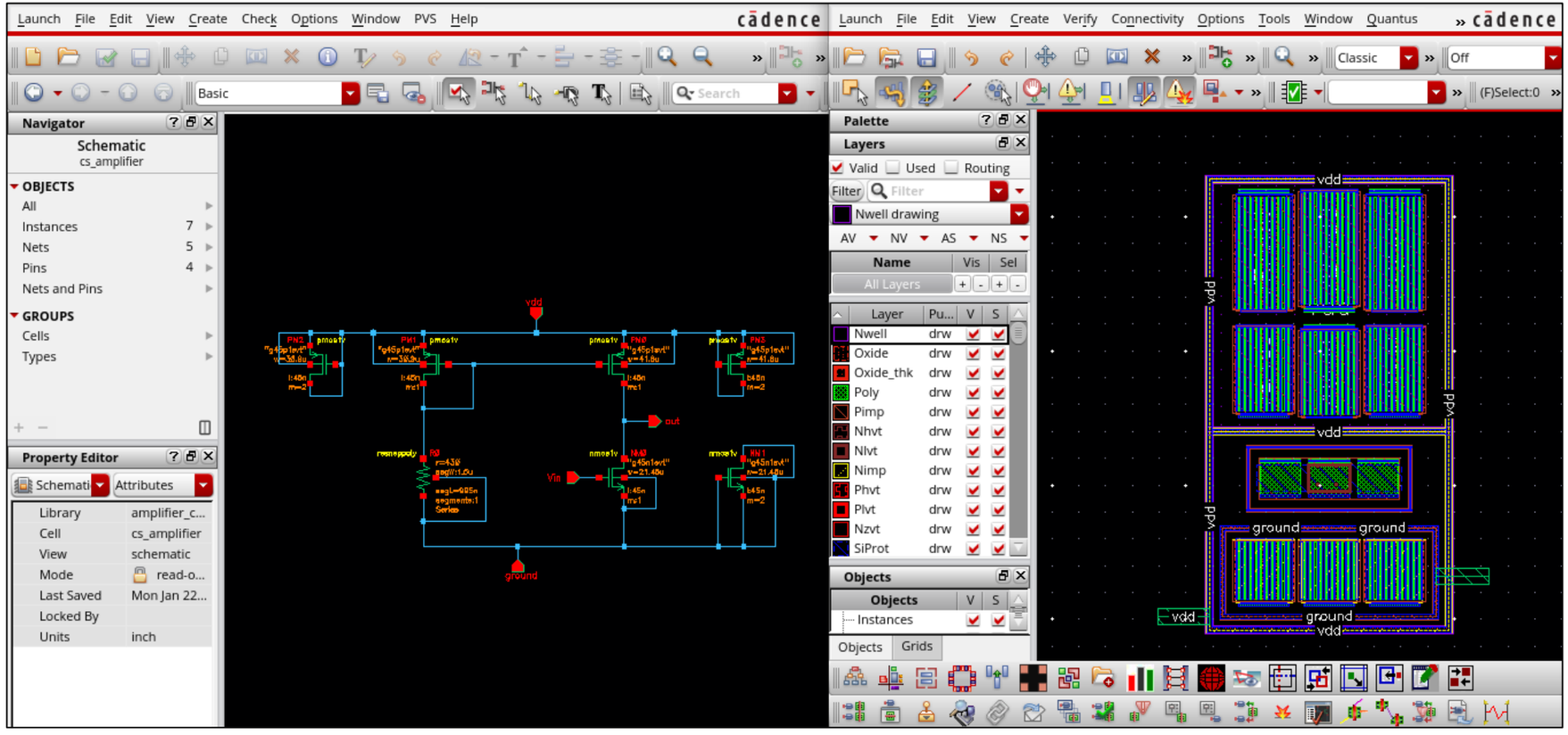
AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

5. Routing the Components *(continued)*

- We will start by routing the NMOS transistors.
- It is recommended to have the schematic next to the layout to make the routing easier.

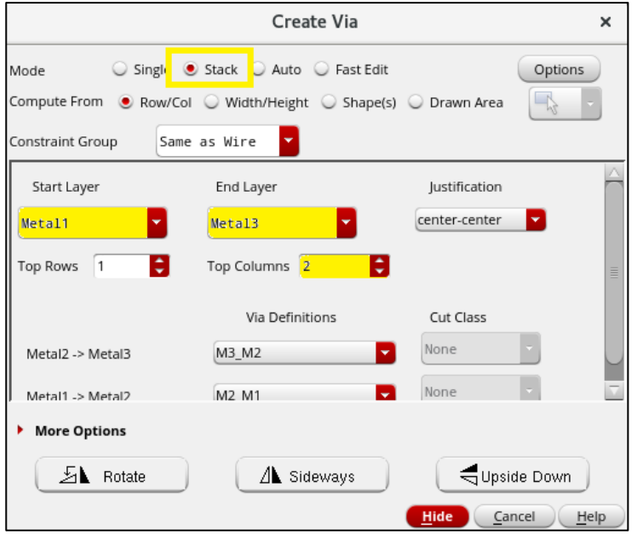


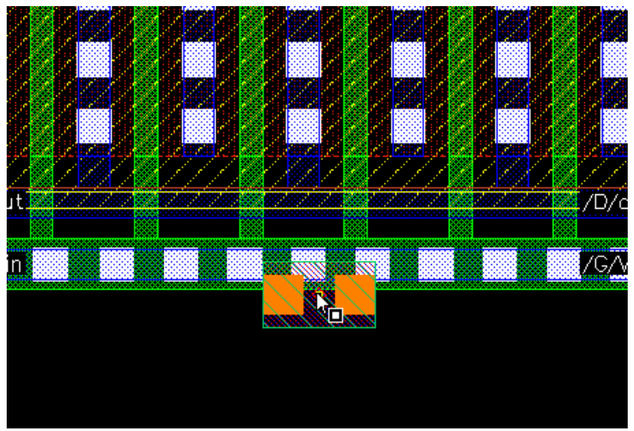
- You can use features like Net Highlighting and Dimming. From the schematic toolbar, Edit → check Net Highlighting and Display Dimming.
- From the layout, Options → Display and check Enable Dimming.

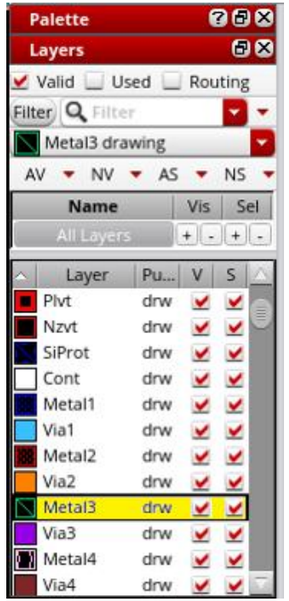
cadence

5. Routing the Components *(continued)*

- First, we will connect the pin Vin to the gate of the transistor.
- Select Metal3 from the Layer Selection Window (LSW).
- Since we are using Metal3 for the path, we need to set up a Metal1 to Metal3 via on the NMOS gate before constructing the path.
- To create a via, from the toolbar, Create → Via… (or O on the keyboard).
- Select **Stack** in mode, then **Metal1** as the Start Layer and **Metal3** as the End Layer.
- Set the columns to 2 and keep the number of rows at 1.



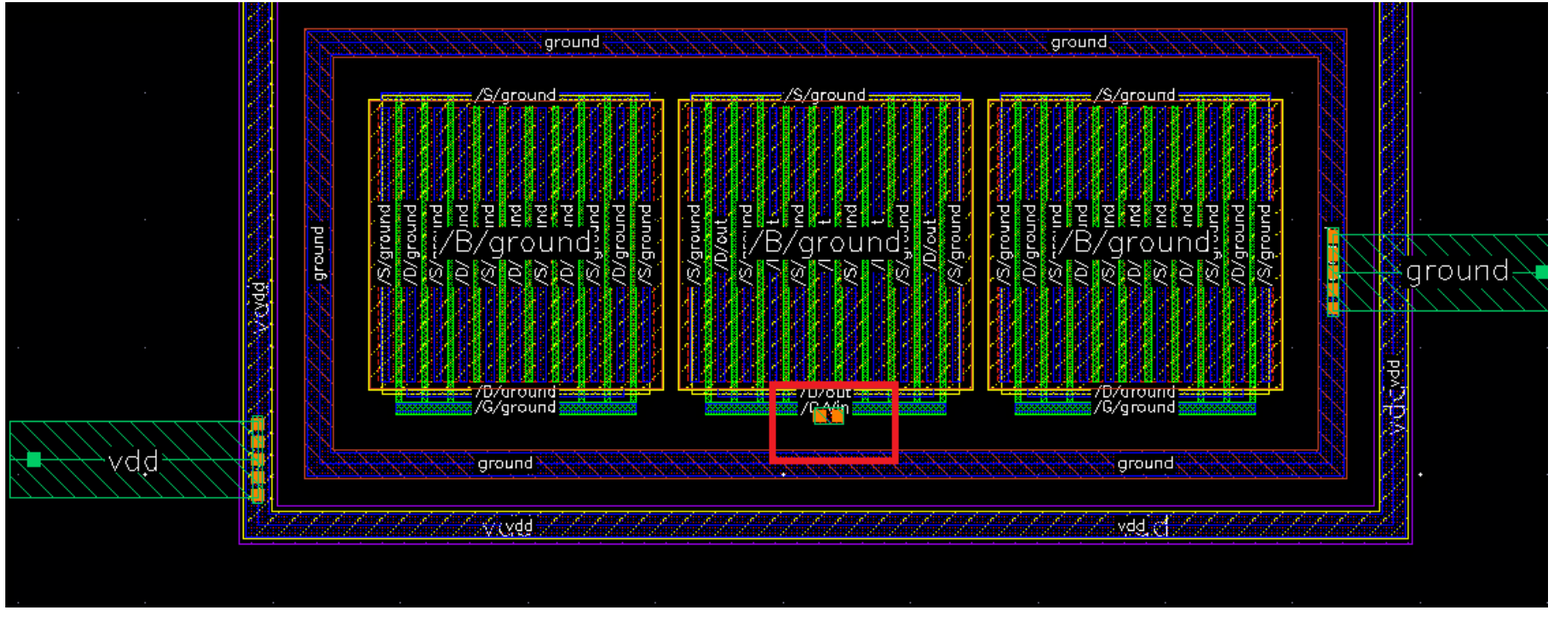




AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

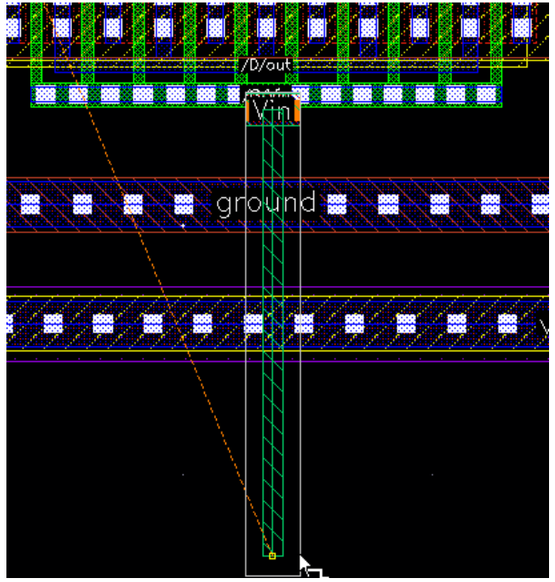
5. Routing the Components *(continued)*

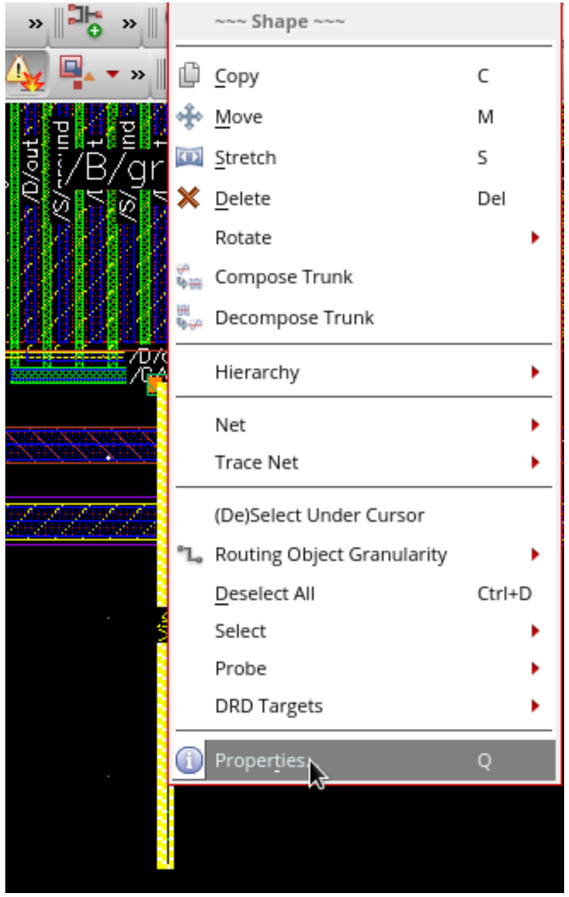


cadence

5. Routing the Components *(continued)*

- To create a path, from the toolbar, Create → Shape → Path (or P on the keyboard). Draw a path from the via on the gate of the NMOS and press enter to confirm the path.
- Right click on the path, then select Properties, or Press Q on your keyboard. Set the Width to 0.6.

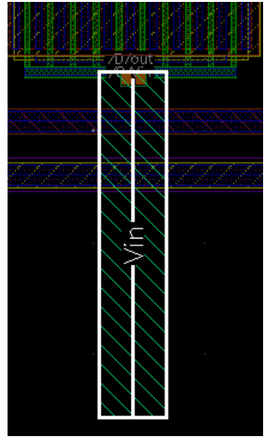




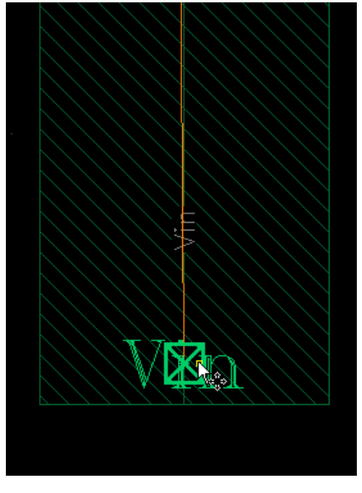
cadence

5. Routing the Components *(continued)*

- The Path should look like this.



- Select the pin Vin from the schematic, it should be highlighted in the layout. Select (you can use Shift to select multiple objects) both the pin Vin and its **label** (Display → Options → Enable Pin Names) and place it on the path as shown here.

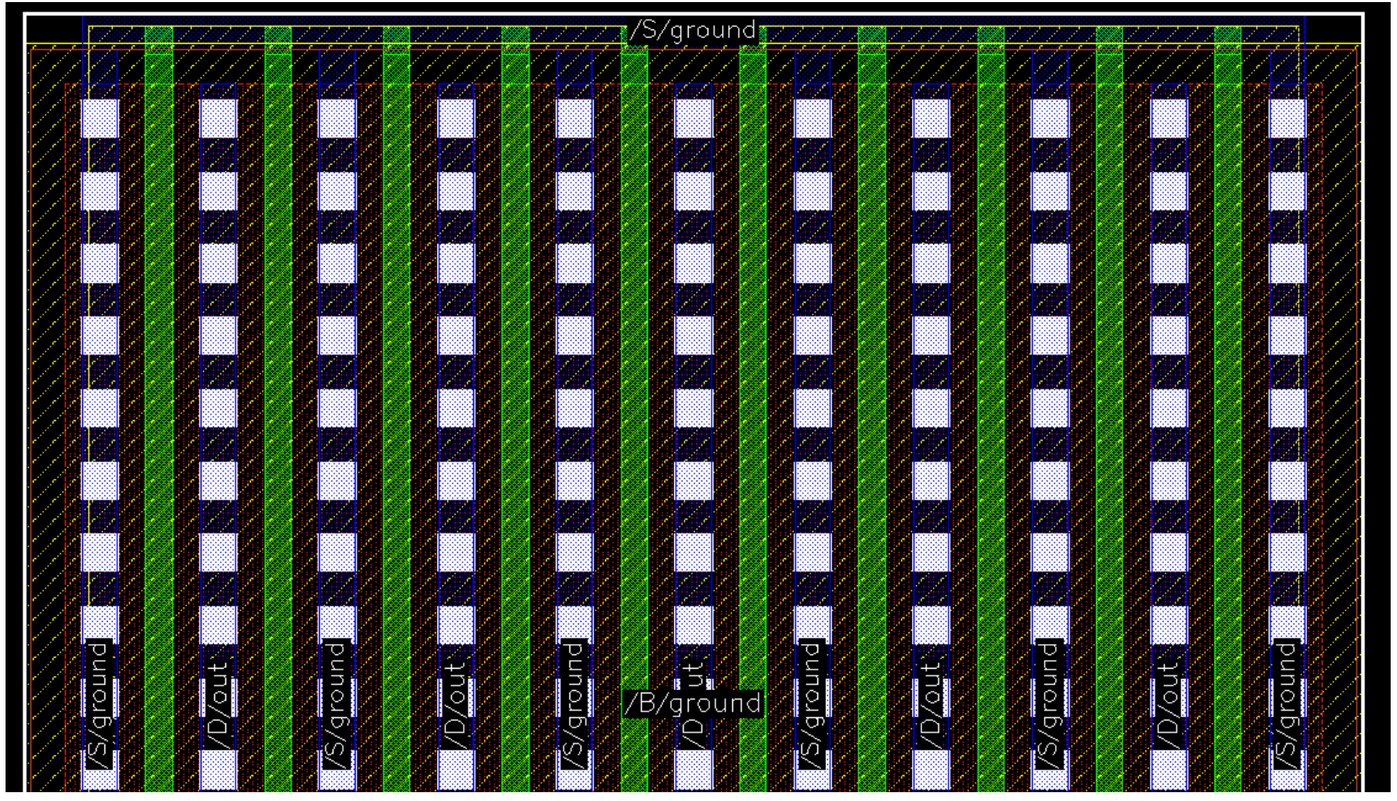


AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

5. Routing the Components *(continued)*

- As you can see from the schematic, the source of the NMOS transistor is connected to ground. Also, the dummy NMOS has all its terminals connected to ground.
- You can zoom in on the transistor to figure out where are the terminals.



- You can use features like Net Highlighting and Dimming. From the schematic toolbar, View→ check Net Highlighting and Display Dimming.
- From the layout, Options → Display and check Enable Dimming.

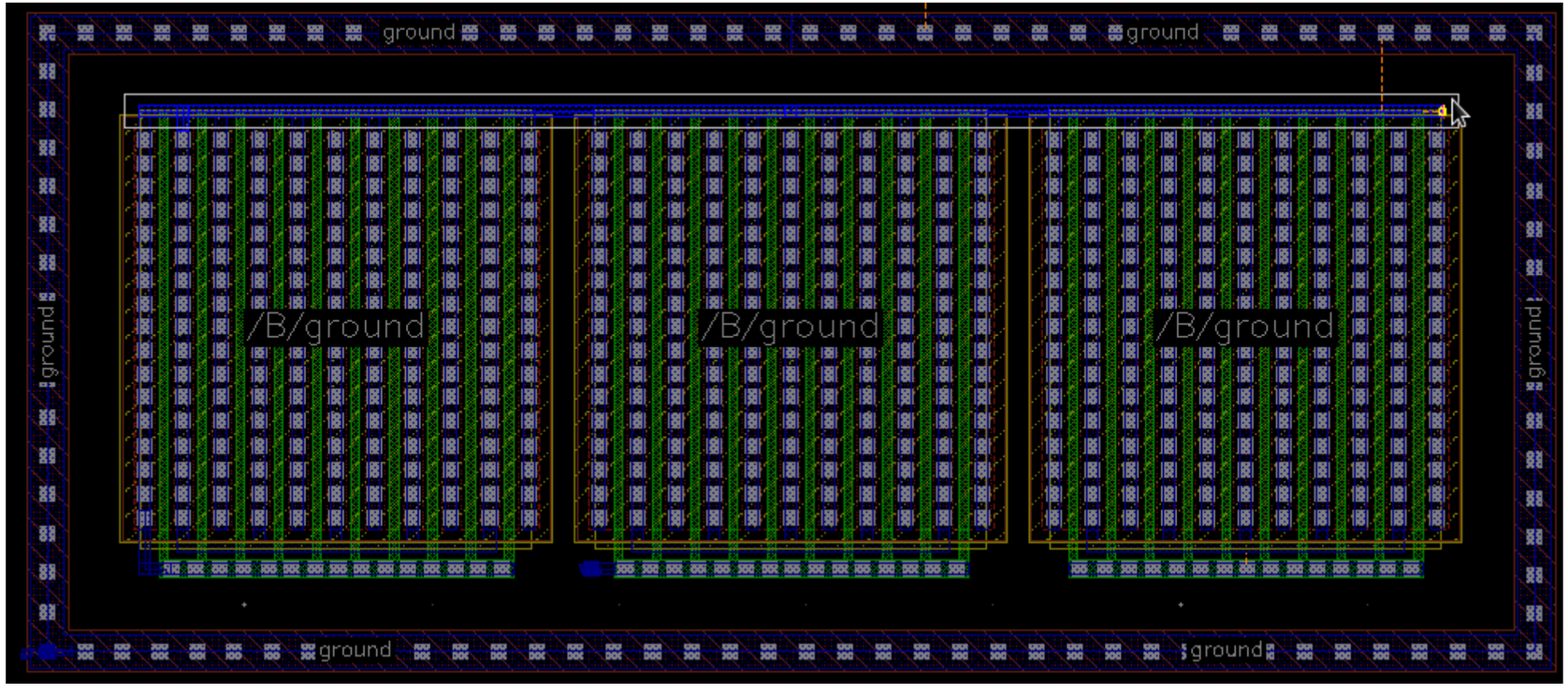
cadence

AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

5. Routing the Components *(continued)*

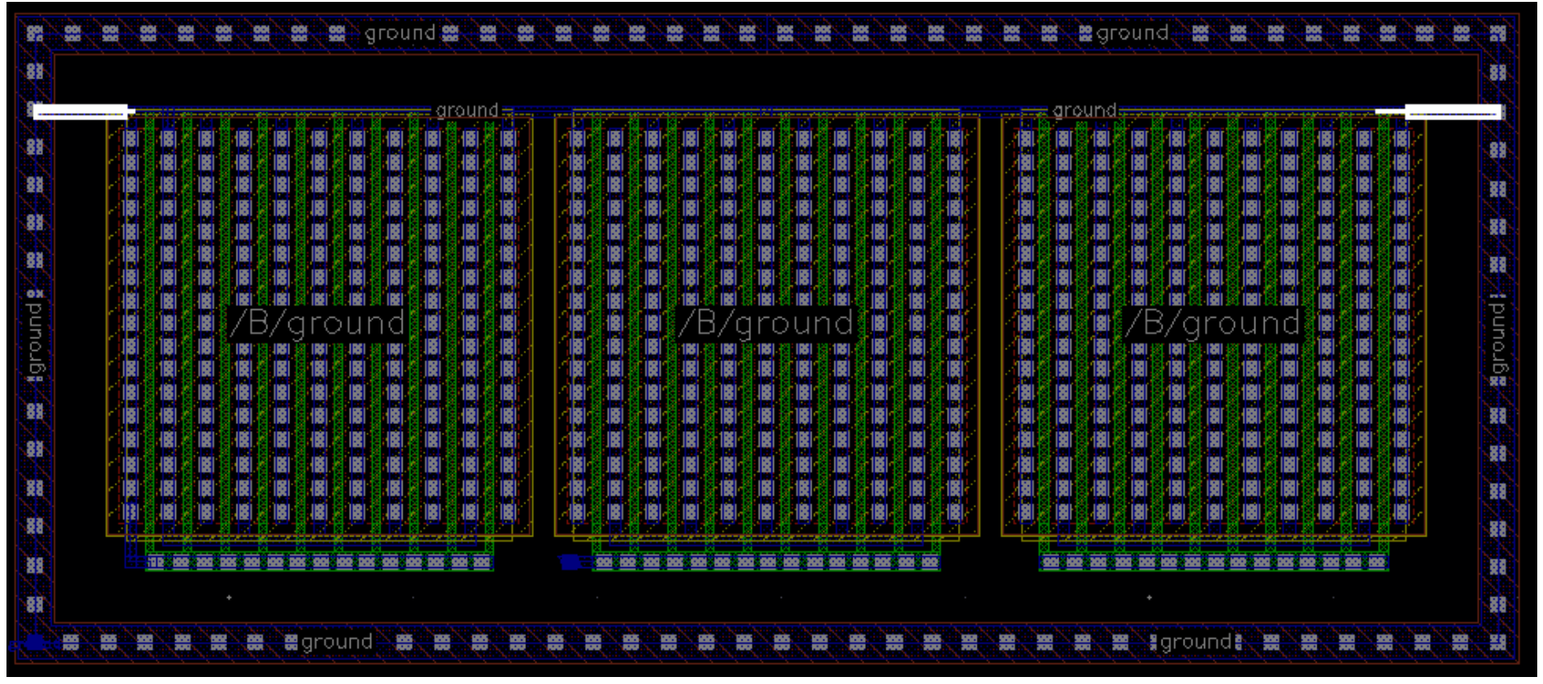
- Select Metal1 from the LSW. Create a path (you can also create a wire under Create => Wiring => Wire) and connect the source of the dummy NMOS transistor to the source of the other dummy NMOS transistor. This connection also connects the source of the NMOS transistor of the actual design to the source of the dummy transistors. The connection is shown below.



cadence

5. Routing the Components *(continued)*

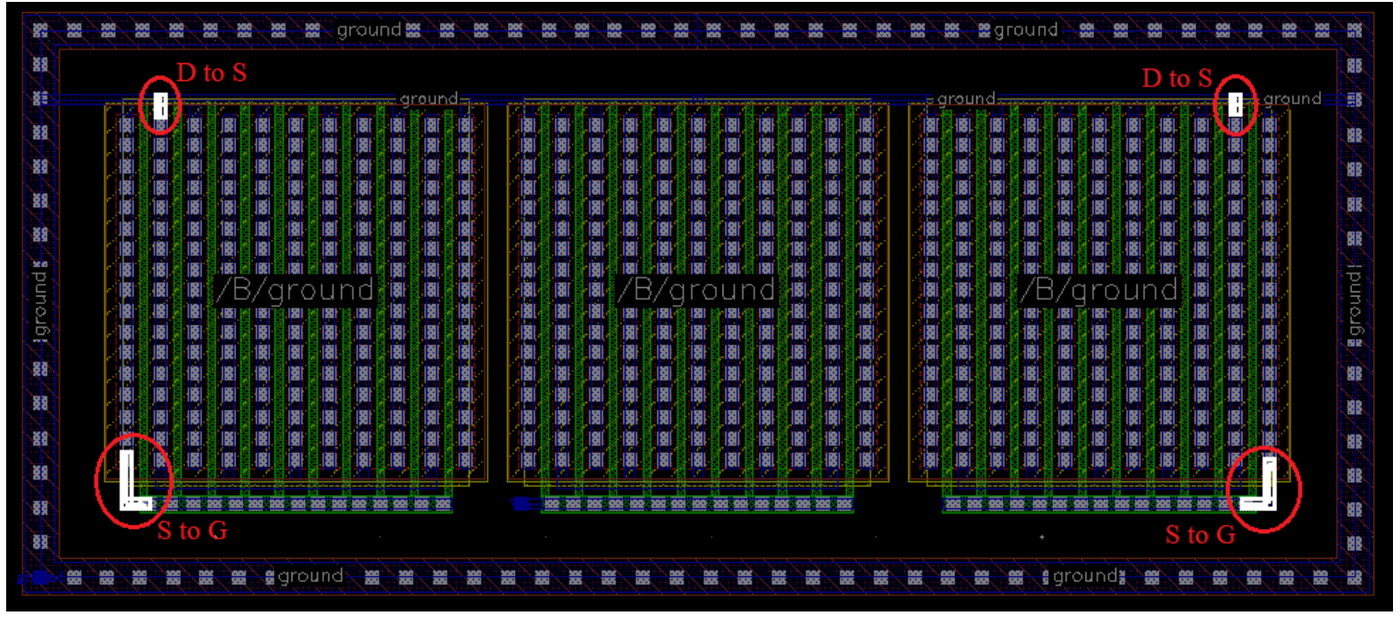
- Add the additional paths on the sides as shown below to connect the sources of the three NMOS transistors to ground.



cadence

5. Routing the Components *(continued)*

- Create a path between the source (S) and the gate (G), also between the drain (D) and source (S) of the dummy transistors.

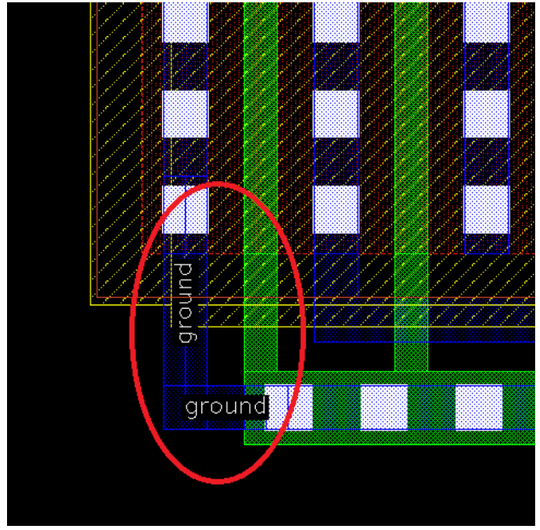


- Notice the connections are done for both dummy devices.

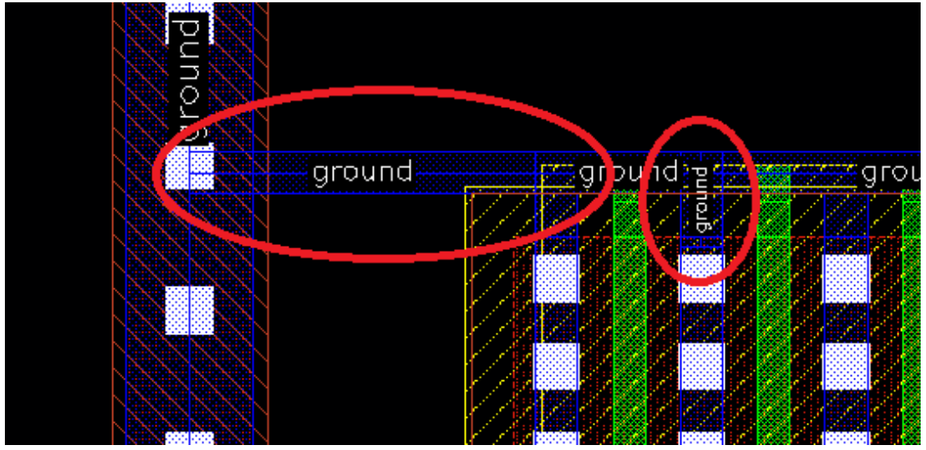
cadence

5. Routing the Components *(continued)*

- Zoomed in view of the connections.



Source to Gate connection



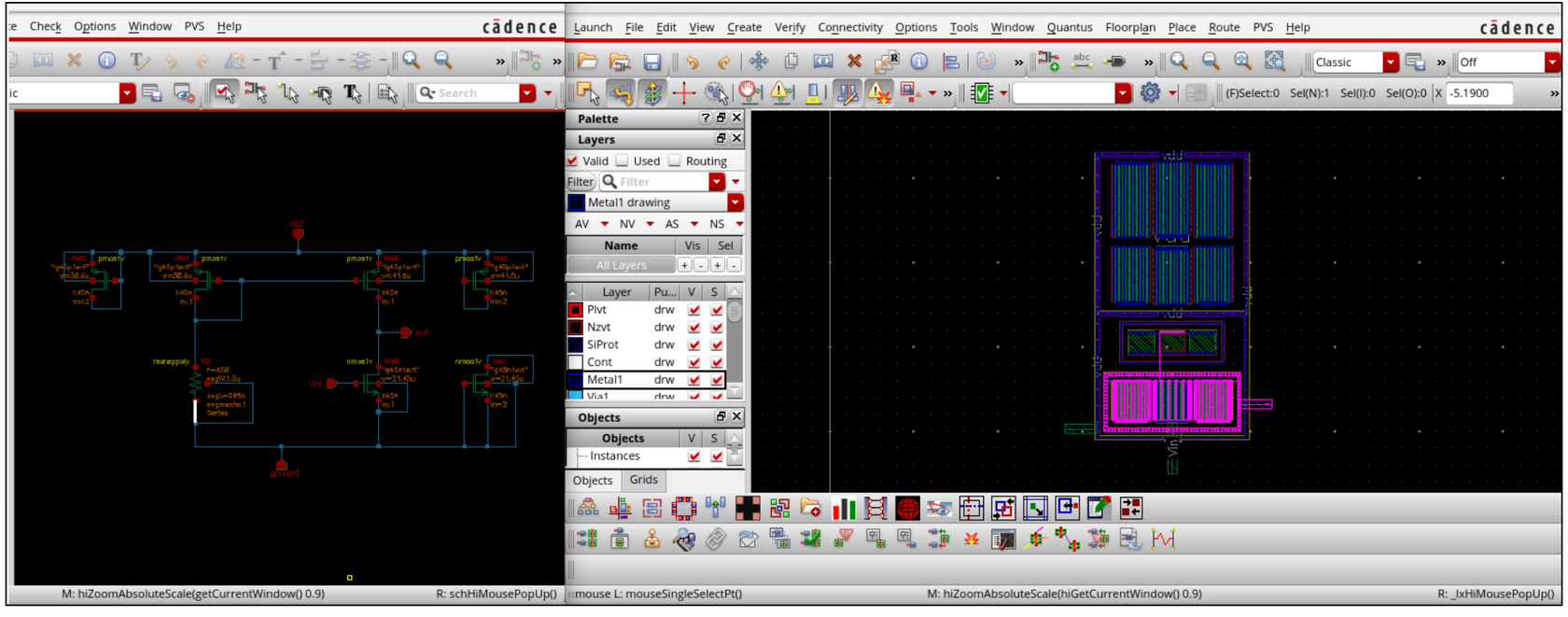
Drain to Source and Source to ground (bulk) connection.

- The following terminals have been connected:
  - Both dummy NMOS transistors: Source, Drain, and Gate
  - NMOS transistor: Source and Gate
- The Drain of the NMOS transistor is connected to the Drain of the PMOS transistor, which in turn is connected to the output pin. This connection will be done later.

cadence

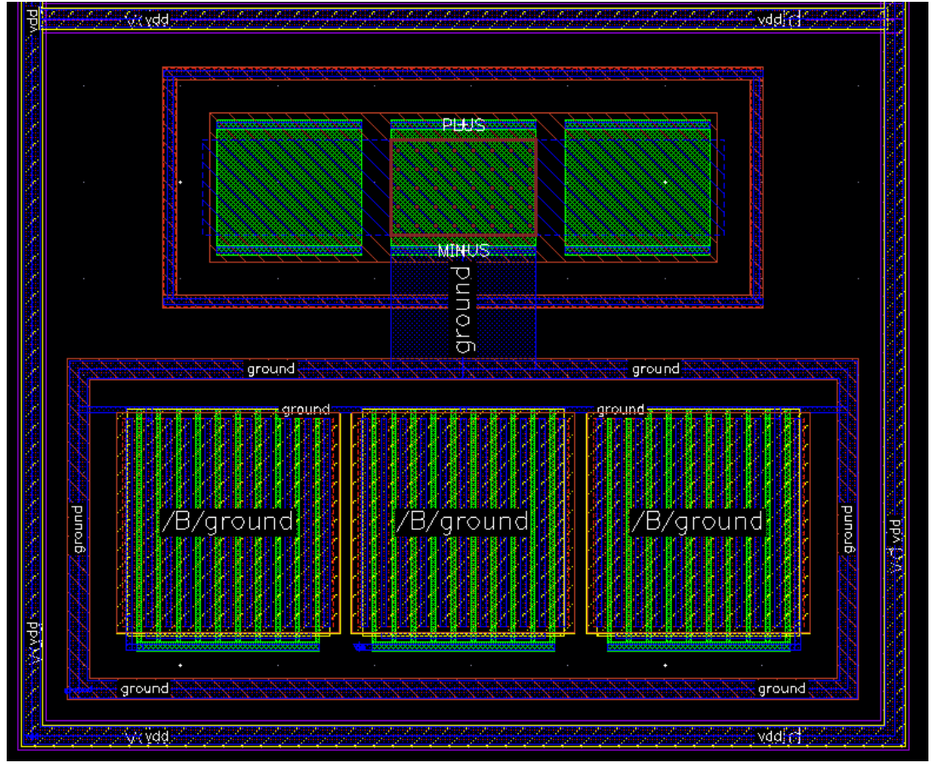
5. Routing the Components *(continued)*

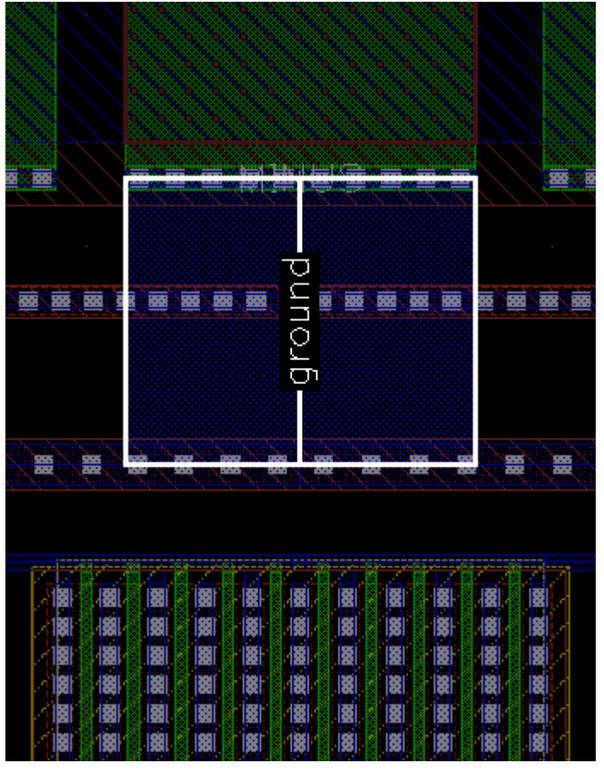
- We will now connect both terminals of the resistor. The plus terminal of the resistor is connected to the Drain of the PMOS transistor and the minus terminal to the ground.
- You can click on the connection to the ground in the schematic to highlight the connection needed to draw in the layout. The figure below shows the highlighted connection. To make the connection shorter, we can flip the resistor vertically. **Select the resistor in the layout, right-click, and select Rotate → Flip Vertical.**



5. Routing the Components *(continued)*

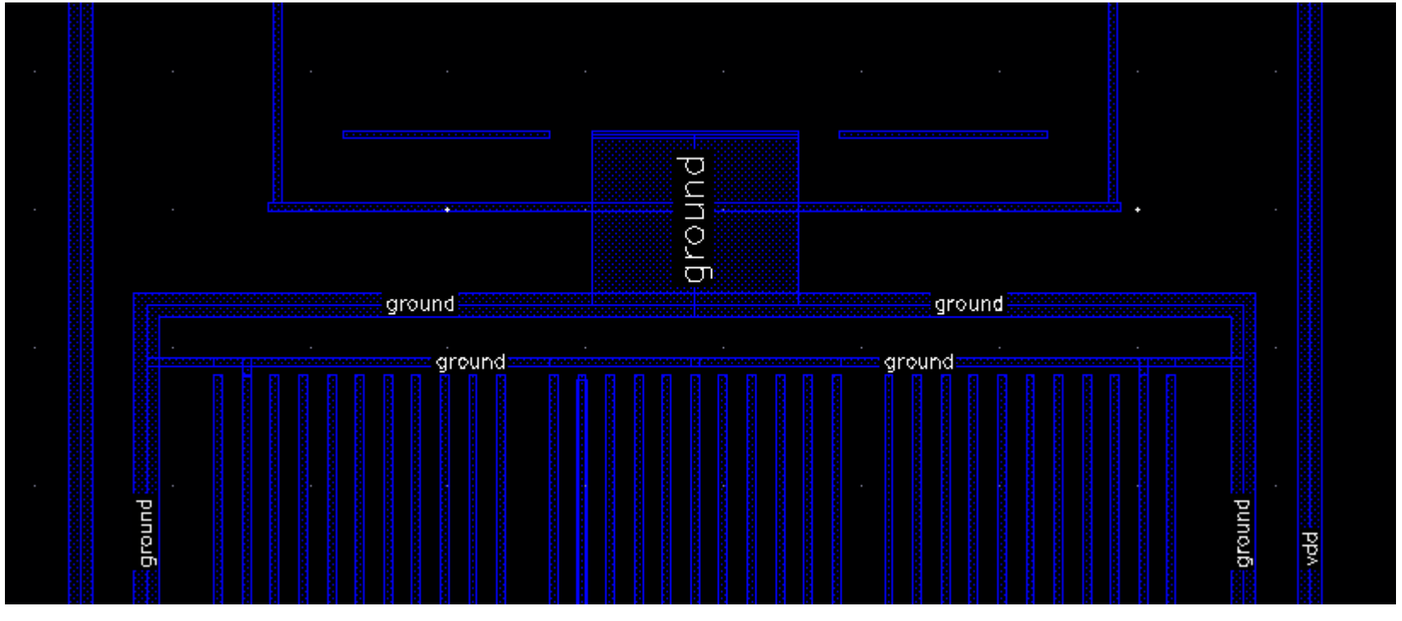
- Select Metal1 from the Layer Selection Window and create a path from the minus terminal of the resistor to the bulk of the NMOS transistors. This connection will also connect the third terminal (bulk) of the resistor to the ground, since the bulk of the resistor contains a Metal1 Layer.
- The connection is shown below.

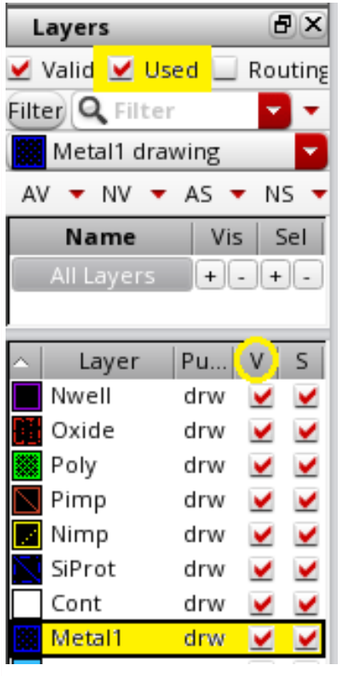




5. Routing the Components *(continued)*

- The connection can further be clearly shown by the following steps.
- Select “Used” from the LSW to only show the layers that have been used in the layout.
- Select the **Metal1** layer from the LSW.
- Click on “V” in the Layers panel to turn off the visibility of the layers except Metal1.
- The connection Metal1 from the minus terminal of the resistor is in contact with the Metal1 layer of the bulk of the NMOS transistor.





cadence

AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

5. Routing the Components *(continued)*

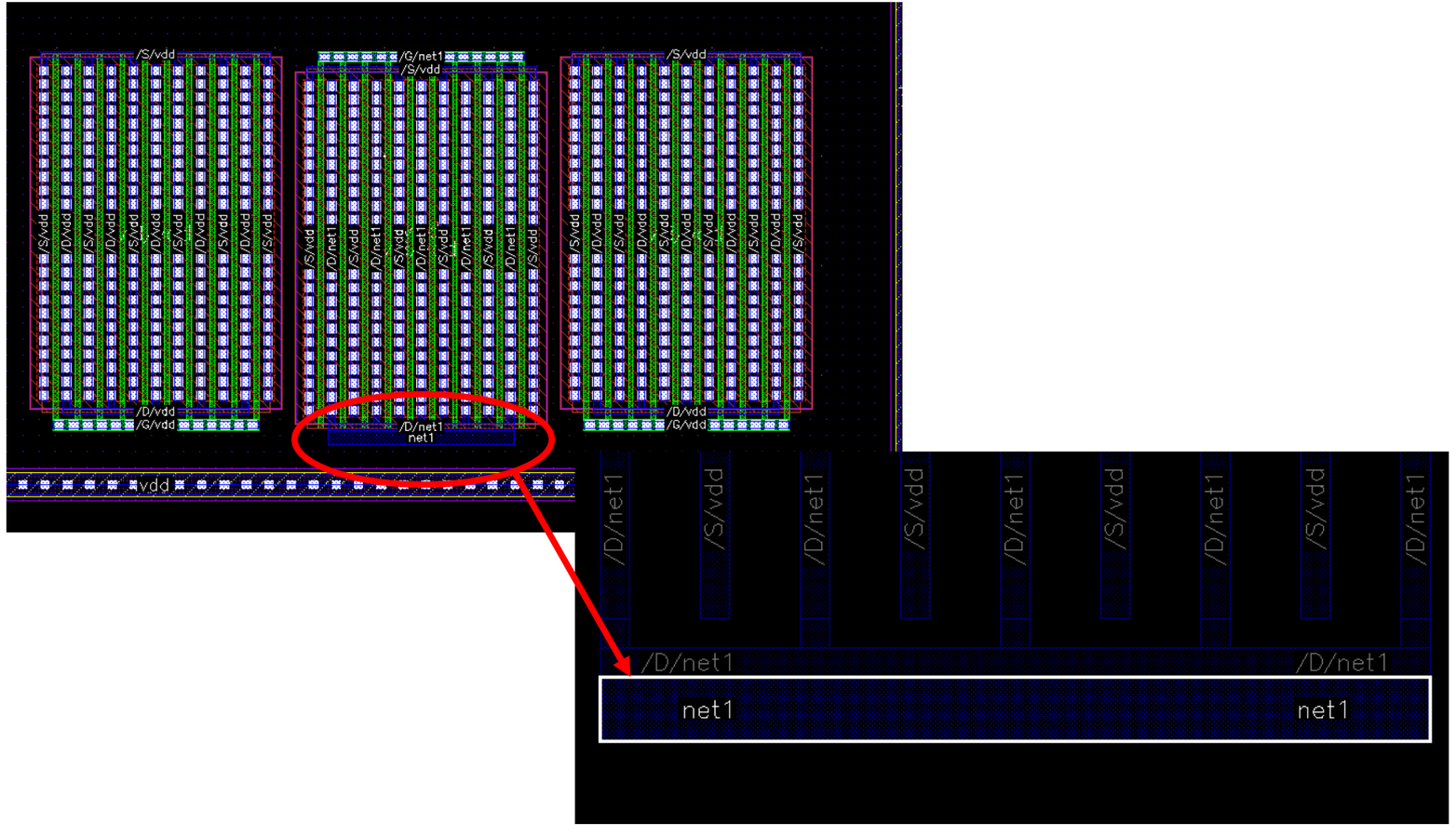
- In order to connect the Drain of the PMOS transistor to the plus terminal of the resistor, we need to use Metal2 layer.
- The bulk of the PMOS transistor and the bulk of the resistor contain a Metal1 Layer, and if the connection was done using a Metal1 layer, it would cross the both bulks, thus creating a short.
- When different metal layers cross each other, a connection is not made unless a Via stack is used.
- A via M2_M1 (Metal2 to Metal1) is needed to move from Metal1 to Metal2.
- First, select Metal1 from the LSW. From the toolbar, Create → Shape → Rectangle (or press R on the keyboard) and create a rectangle connecting the drain of the PMOS as shown on the next slide.
- You can align the edges by using the Stretch feature. From the toolbar, change the selection mode from Full Select  to Partial Select  . Select only the edge of the rectangle that needs to be aligned with the edge of the Drain. Press S on the keyboard (or Edit → Stretch) and make the appropriate modification.
- Select the drawn rectangle, and press Q on the keyboard (or right-click and Properties) to open the Edit Rectangle Properties form.
- Change the Height to 0.13, and make sure the Width is 1.7 (width of the drain rectangle).

cadence

AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

5. Routing the Components *(continued)*

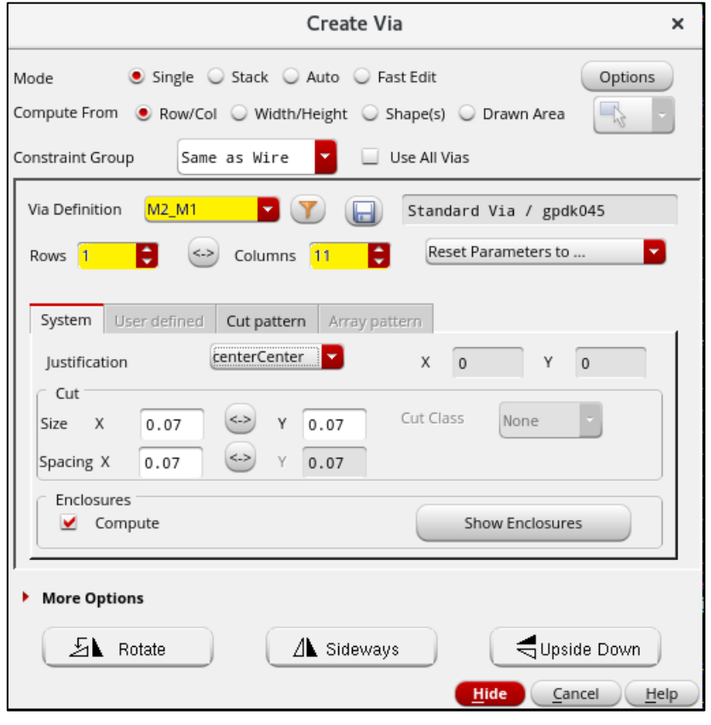


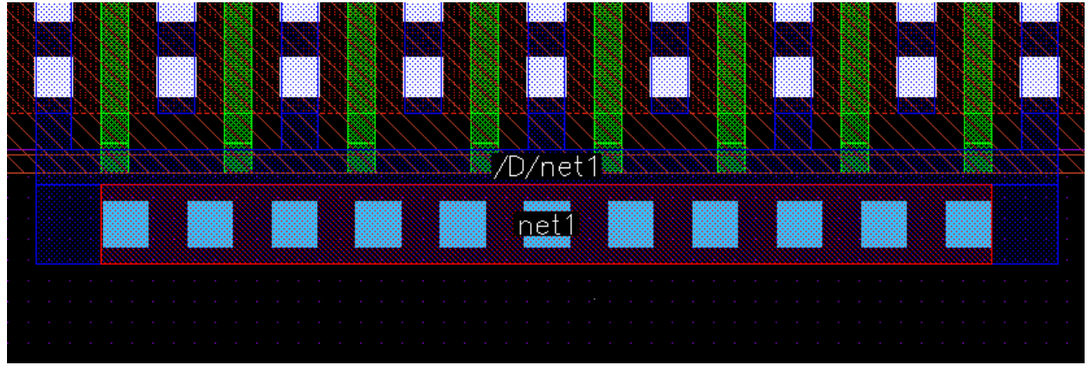
- Notice how the rectangle, is aligned from both sides to the rectangle of the Drain.
- We must align the edges in order not to face errors later when we run DRC.

cadence

5. Routing the Components *(continued)*

- The next step is to add the Metal2_Metal1 Via on top of the drawn rectangle.
- From the toolbar, Create → Via (or press O on the keyboard).
- From the drop-down list of Via Definition, select M2_M1. Change the number of Columns to 11 and place the via on top of the drawn rectangle as shown below. Notice how the via also is aligned from the top and the bottom (Edit → Move or press M on the keyboard).

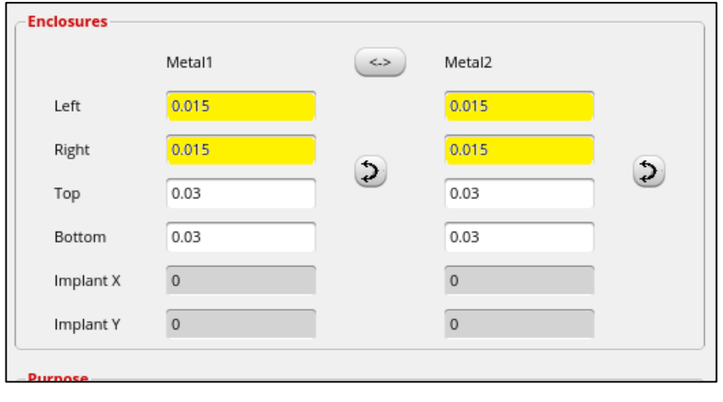


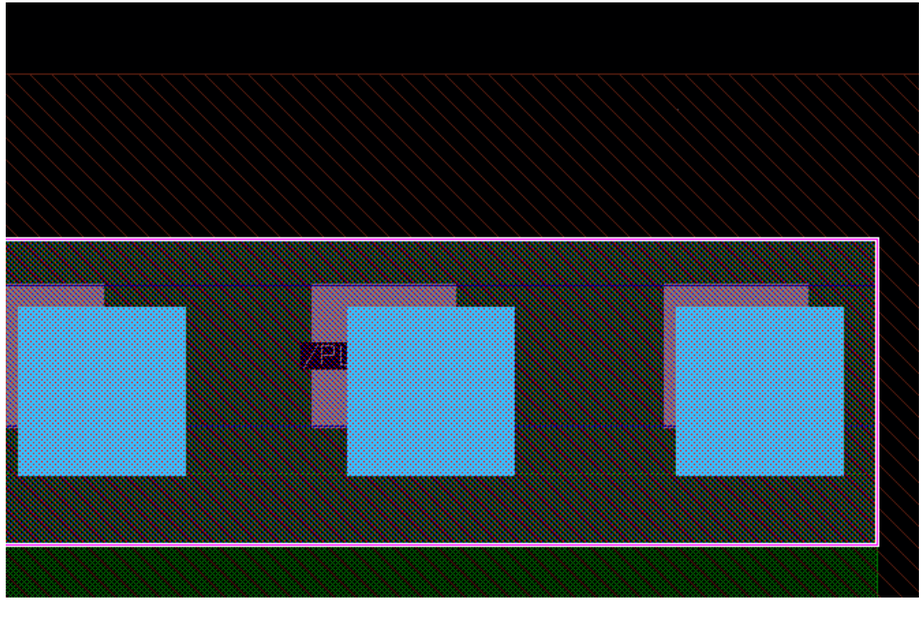


cadence

5. Routing the Components *(continued)*

- Similarly, create a via M2_M1 and place it on top of the plus terminal of the resistor.
- Make sure that the via placed on top of the plus terminal of the resistor aligns perfectly like shown in the figure below.
- To ensure that the via fits exactly, select it, press Q to open its attributes, then adjust the following parameters.
- Next, choose the via and click M to position it correctly.



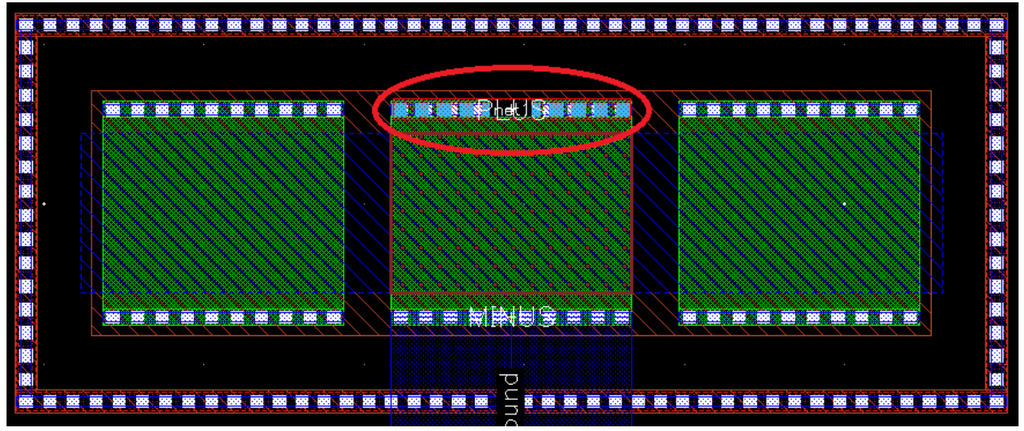


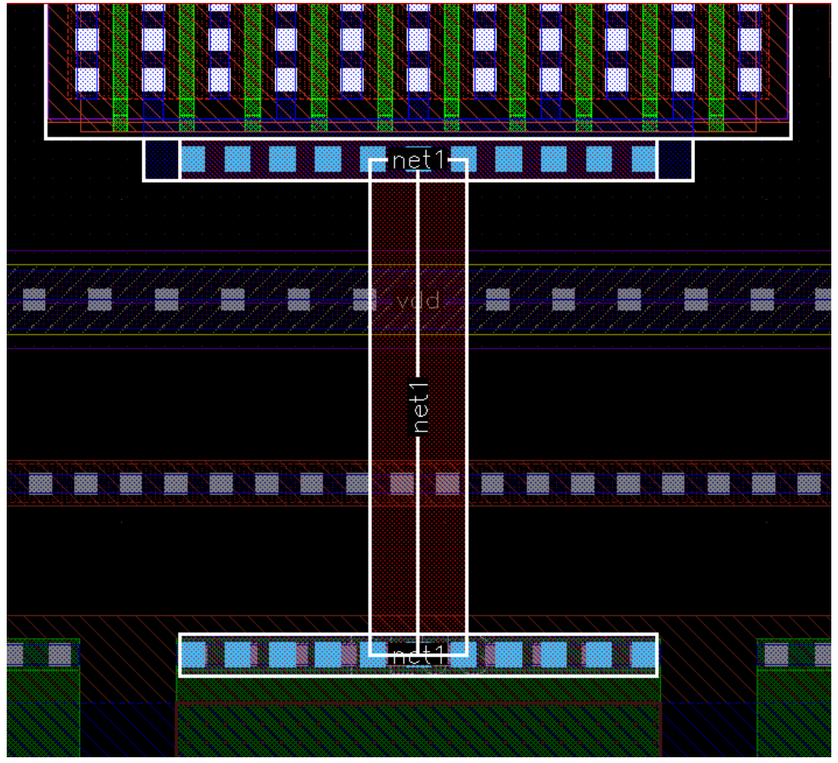
cadence

5. Routing the Components *(continued)*

- Select **Metal2** from the LSW and create a path (P) from one via to the other. This connection connects the drain of the PMOS transistor to the plus terminal of the resistor.

- Select the connection and press Q to open Properties. Change the width of the connection to 0.3.

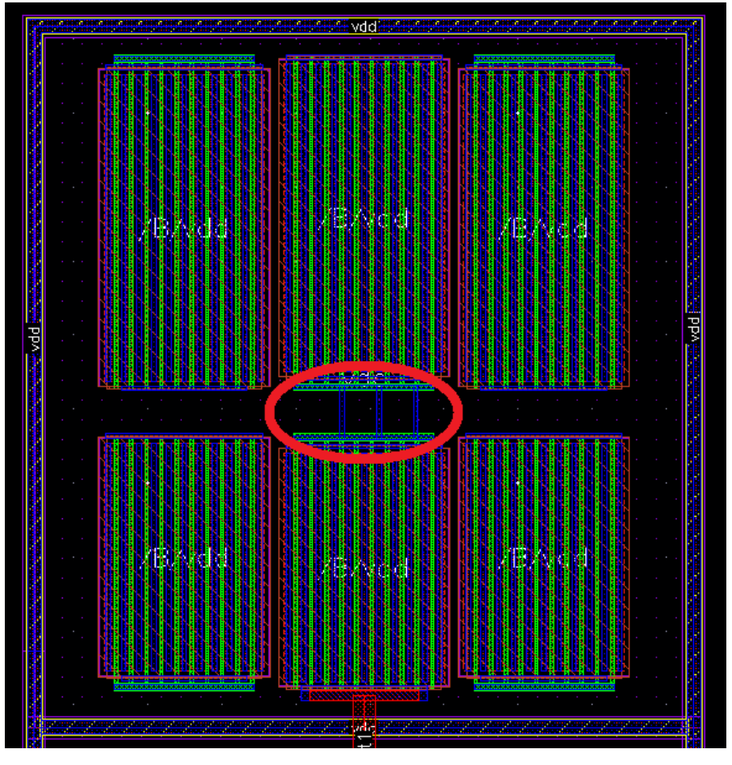


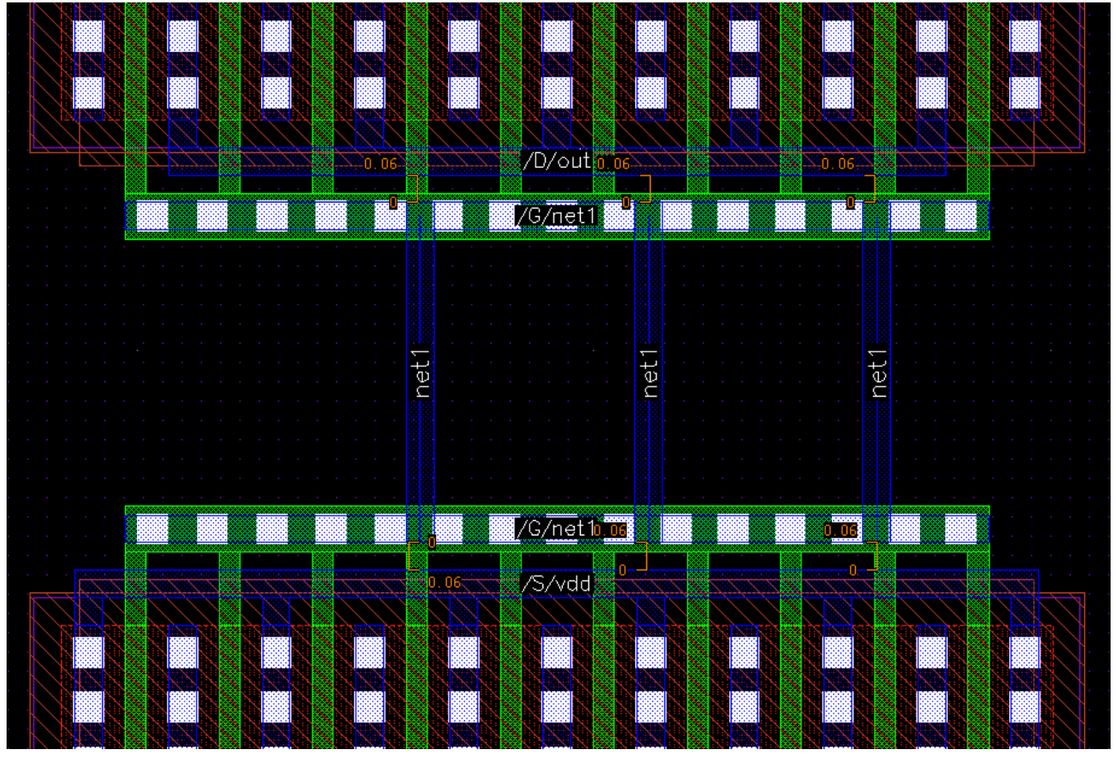


cadence

5. Routing the Components *(continued)*

- The next step is to connect the gates of the two PMOS transistors together.
- Select the layer Metal1 from the LSW. Create multiple paths (P) to connect the gates as shown below. Make sure to have a minimum of 0.06 µm between Metal1 layers.
- The connection is shown below.

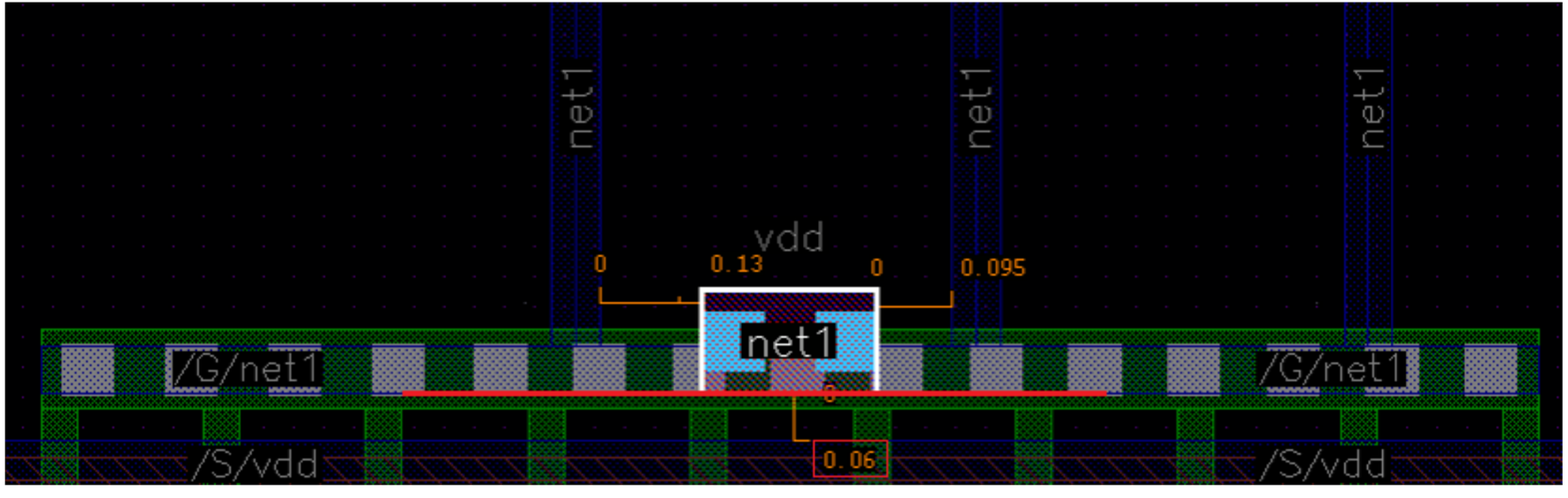




cadence

5. Routing the Components *(continued)*

- The next step is to connect the gate of the PMOS transistor to the drain.
- A via M2_M1 (Metal2 to Metal1) is needed in order not to create a short circuit between the source and the drain of the PMOS transistor.
- From the toolbar, Create → Via (or O), from the drop-down list of Via Definition, select M2_M1. Change the number of columns to 2 and place the via on top of the gate of the PMOS transistor as shown below. Make sure to have a minimum spacing of 0.06 µm between two Metal1 layers (the via contains Metal1 layer).



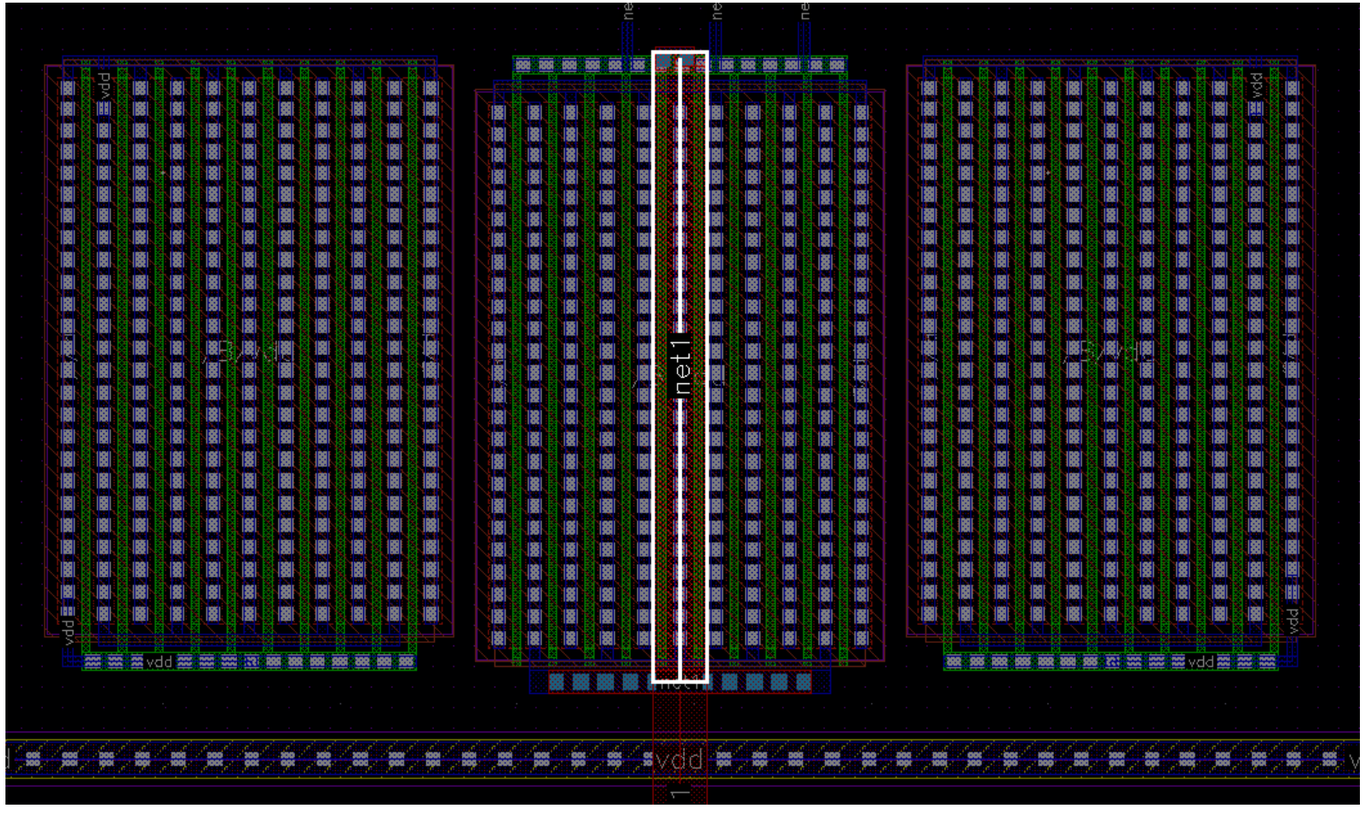
- Note that the measurements in this image need to be at least 0.06 µm. In this case, there is no need to take the exact measurements.

AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

5. Routing the Components *(continued)*

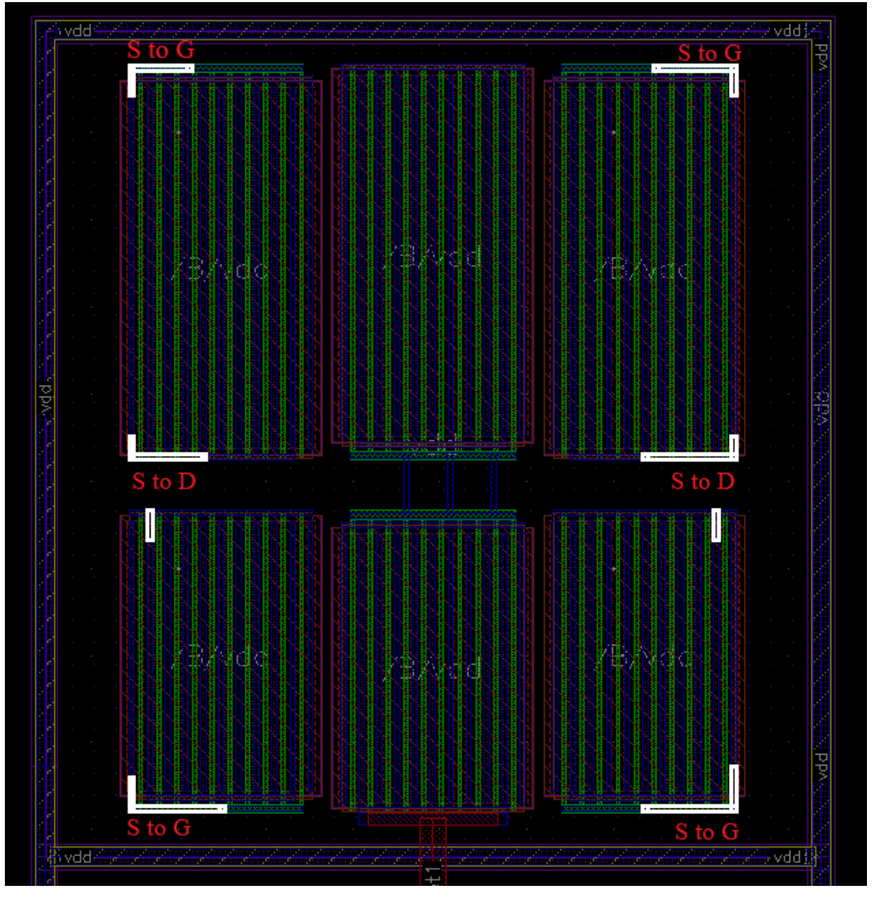
- Select Metal2 from the LSW. Create a path (P) from the drain of the PMOS and connect it to its gate (to the via M2_M1). Select the connection, click Q (properties), and change the width to 0.3.
- The connection is shown below.



cadence

5. Routing the Components *(continued)*

- The next step is to connect the source of PMOS transistors to Vdd.
- Notice that all the terminals of the dummy PMOS transistors are connected to Vdd. Thus, we will connect the source of the PMOS transistor to the source (drain, or gate) of the dummy transistor, and in turn connect the source of the dummy PMOS transistor to Vdd.
- The following connections are needed for the dummy PMOS transistors:
  - Source to Gate connection
  - Drain to Source connection
- Select Metal1 from the LSW.
- Create paths (P) to connect the terminals accordingly.
- The connections are shown in the figure (zoomed-in views are on the next slide). Make sure to connect all four dummy PMOS transistors.



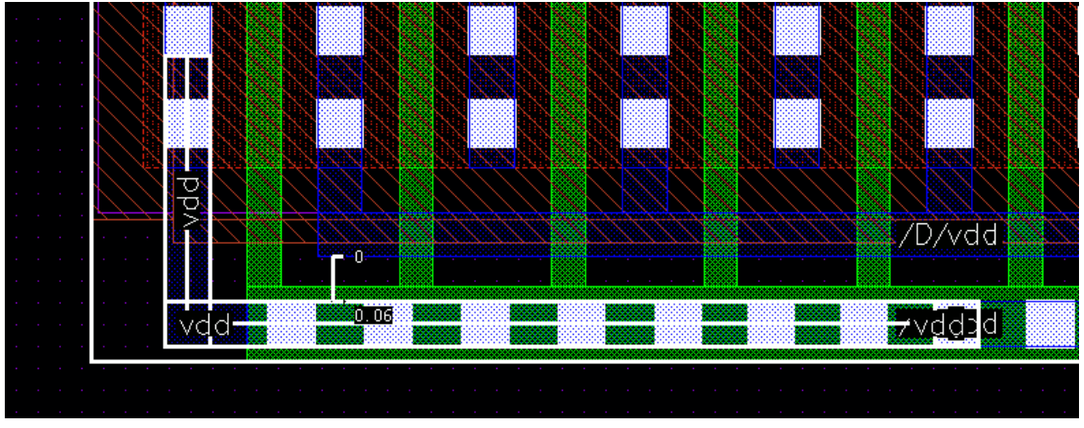
cadence

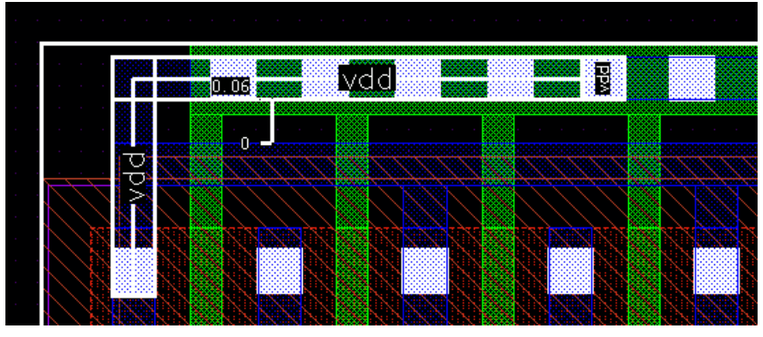
AMERICAN UNIVERSITY OF BEIRUT

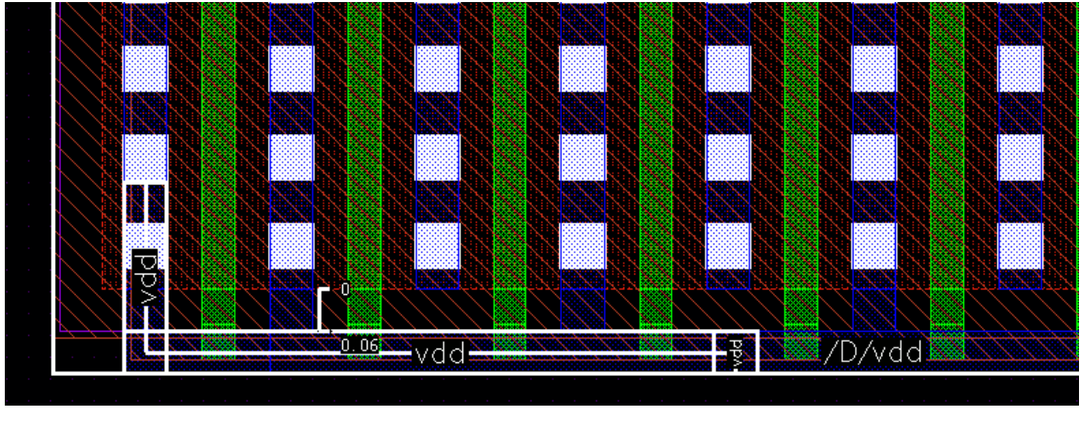
- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

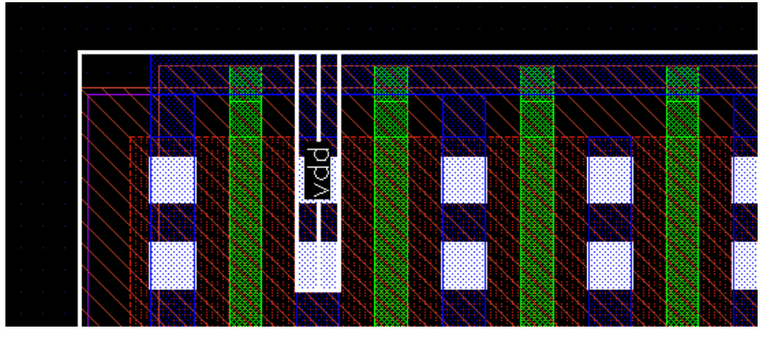
5. Routing the Components *(continued)*

- Make sure to have a minimum spacing of 0.06 µm between two Metal1 layers.
- Zoomed in view of the connections are given below.









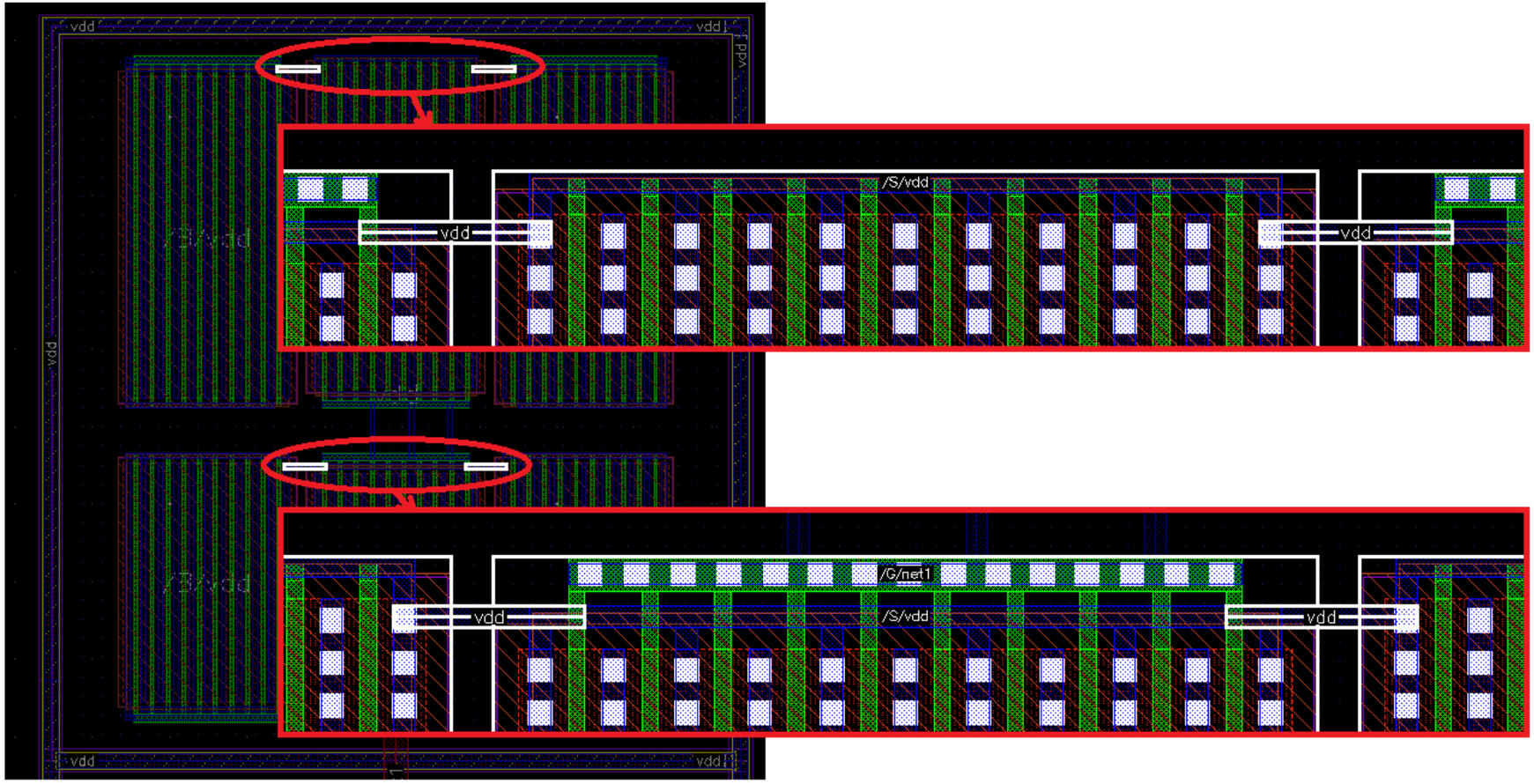
cadence

AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

5. Routing the Components *(continued)*

- Connect the source of the PMOS transistors to the source of the dummy PMOS transistor as shown below using Metal1 layer.



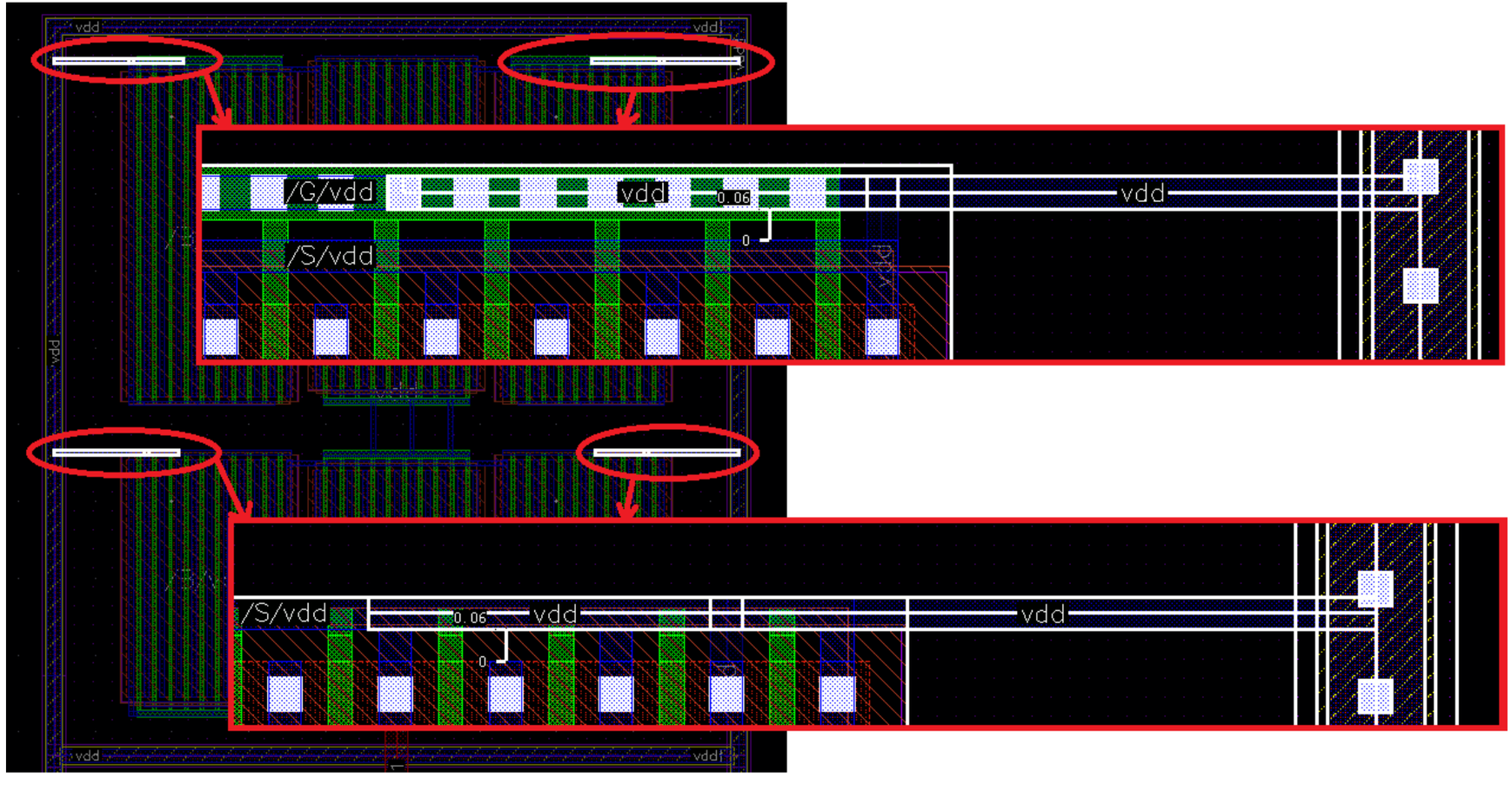
cadence

AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

5. Routing the Components *(continued)*

- Now add the paths (P) from the source to the Vdd (bulk) using Metal1 layer from the LSW.



- Make sure to have a minimum space of 0.06 µm between two Metal1 layers.

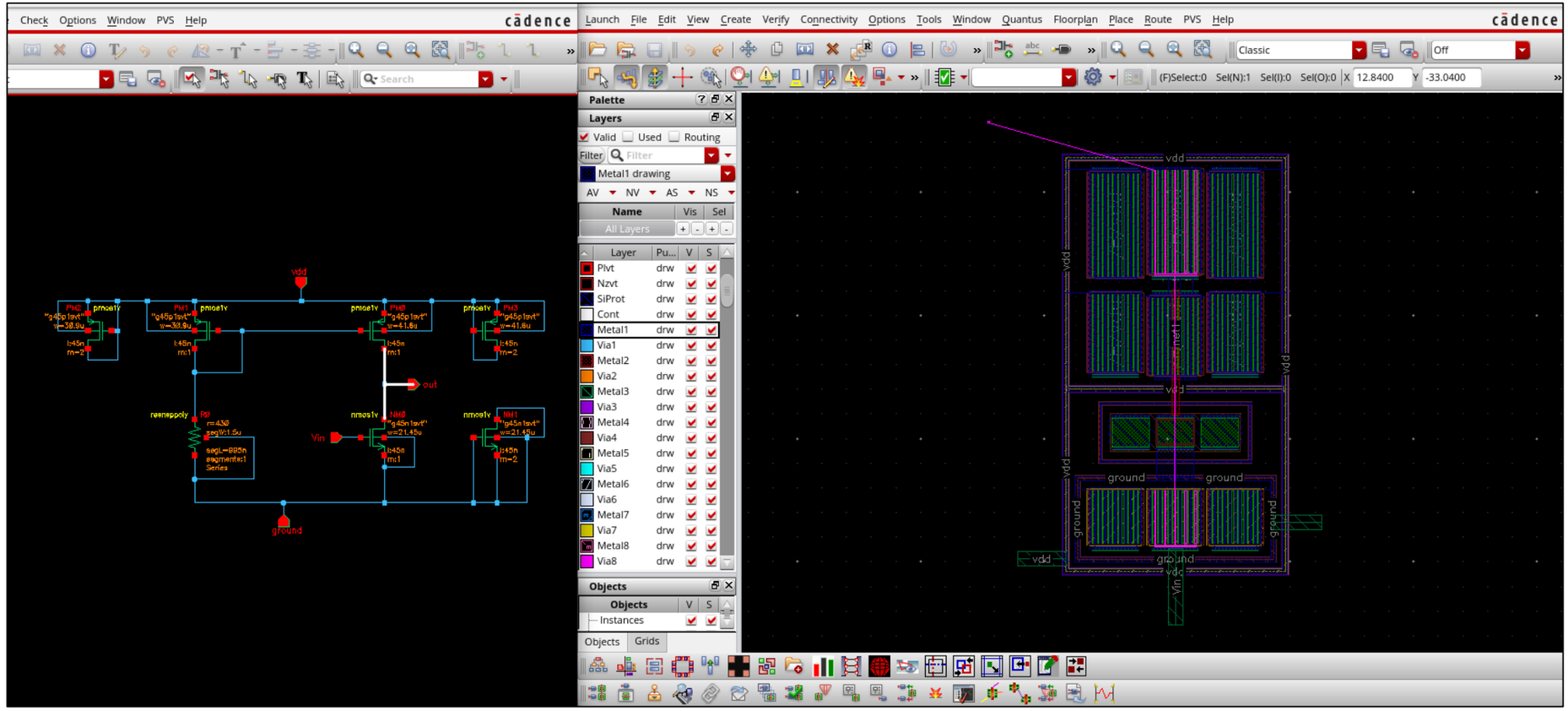
cadence

AMERICAN UNIVERSITY OF BEIRUT

- Adding Dummy Transistors
- Layout MXL Overview
- Generating the Components
- Placing the Components
- Routing the Components

5. Routing the Components *(continued)*

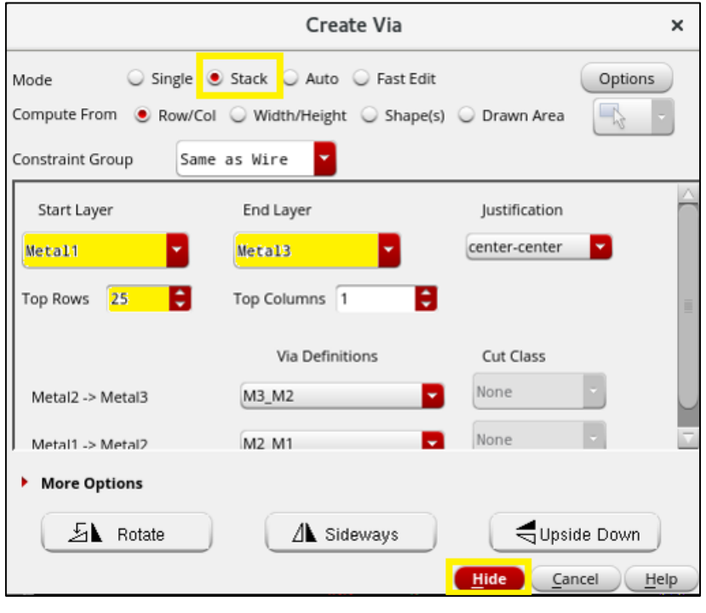
- The last step is to connect the drain of the PMOS transistor to the Drain of the NMOS transistor and connect it to the out pin.

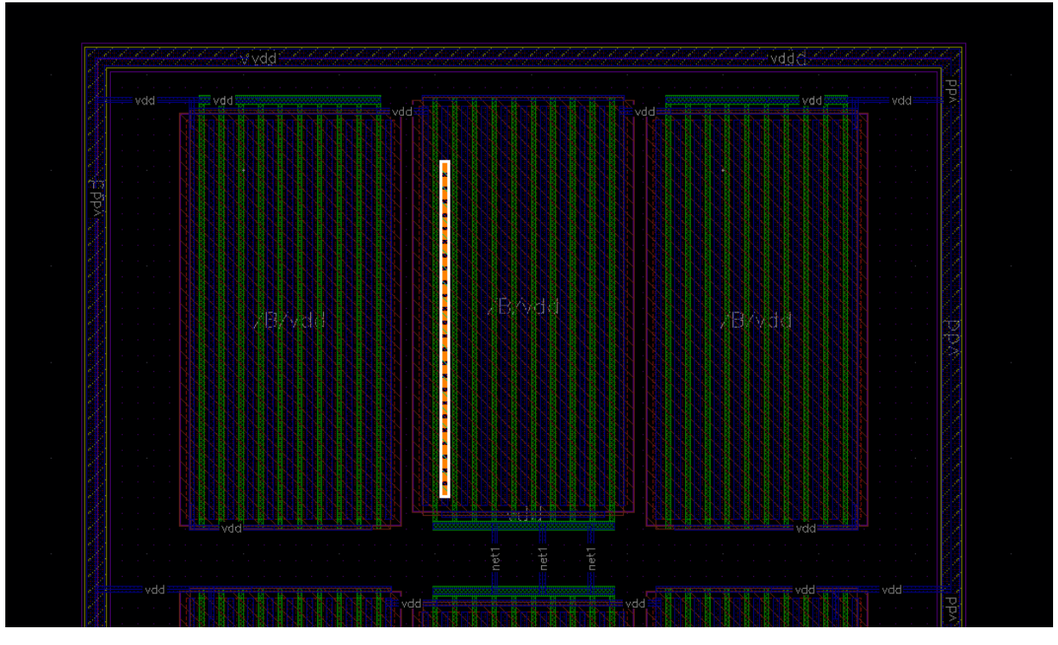


cadence

5. Routing the Components *(continued)*

- We must use vias in order not to make a wrong connection.
- From the toolbar, Create → Via (or press O on the keyboard).
- Choose Stack as the Mode. The Start Layer will be Metal1, since the drains contain a Metal1 layer and the End Layer will be Metal3, since we would like to make sure not to connect to any other connection or device.
- Change the Top Rows to 25, click Hide, and place the via on top of the drain of the PMOS transistor.



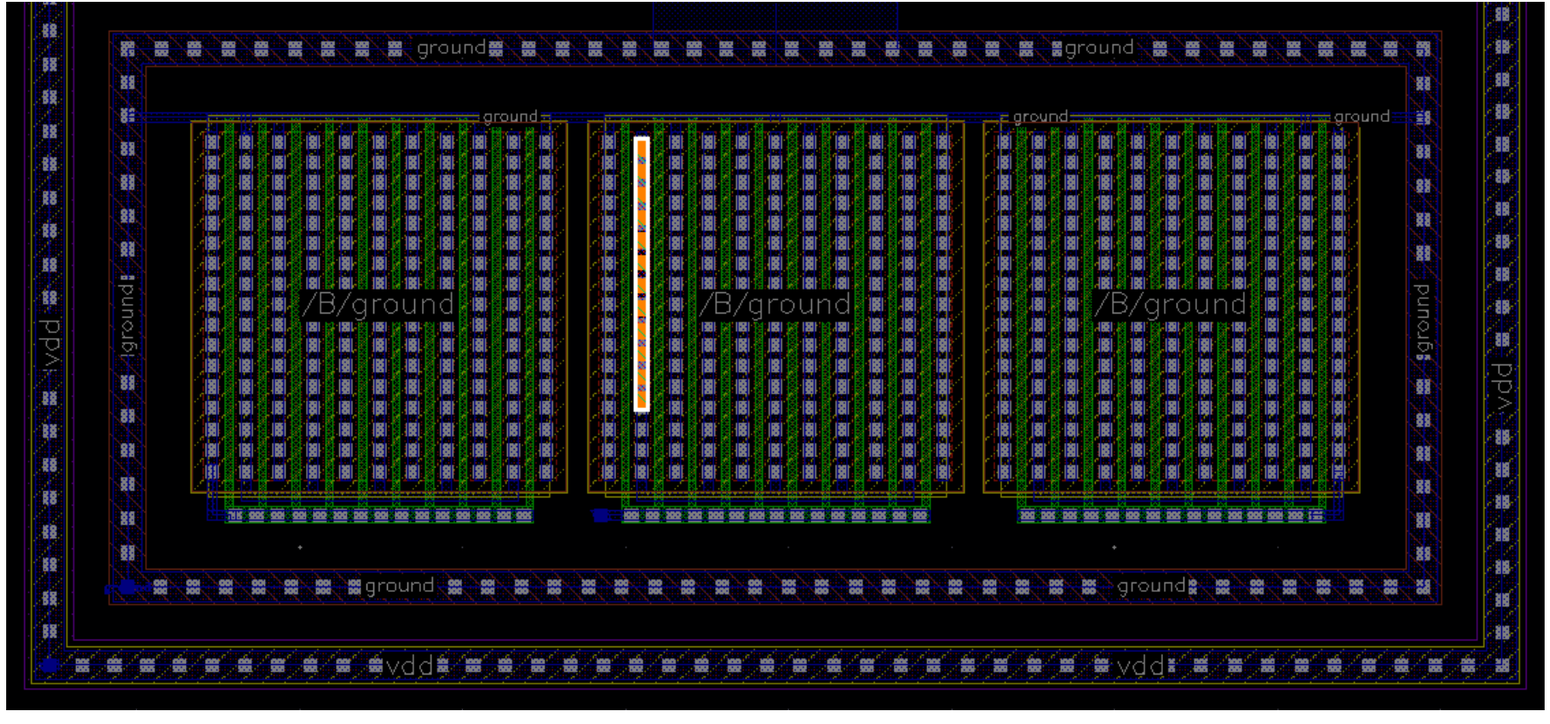


- If you clicked Hide, and want to open the form again, press F3.

cadence

5. Routing the Components *(continued)*

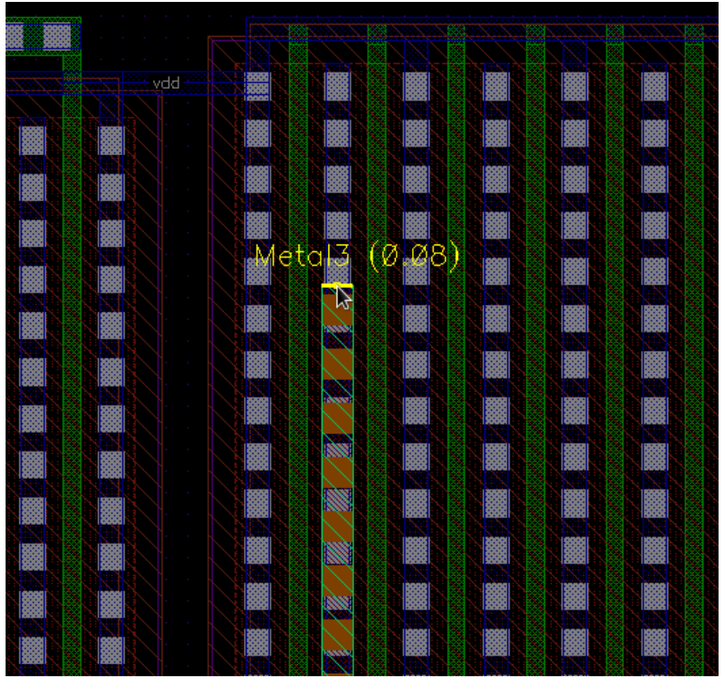
- Create another via stack of Metal1 to Metal3. Change the Top Rows to 12 and place it on top of the drain of the NMOS transistor as shown below.

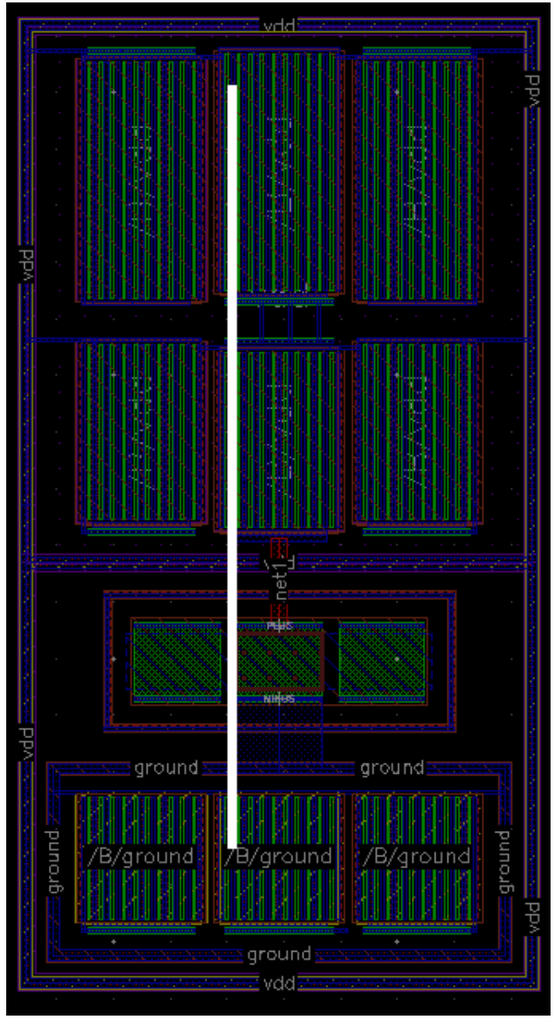


cadence

5. Routing the Components *(continued)*

- Select Metal3 from the LSW. From the top edge of the via placed on top of the drain of the PMOS transistor, create a path (P) and connect it to the via placed on top of the drain of the NMOS transistor.
- The figure shows the connection.





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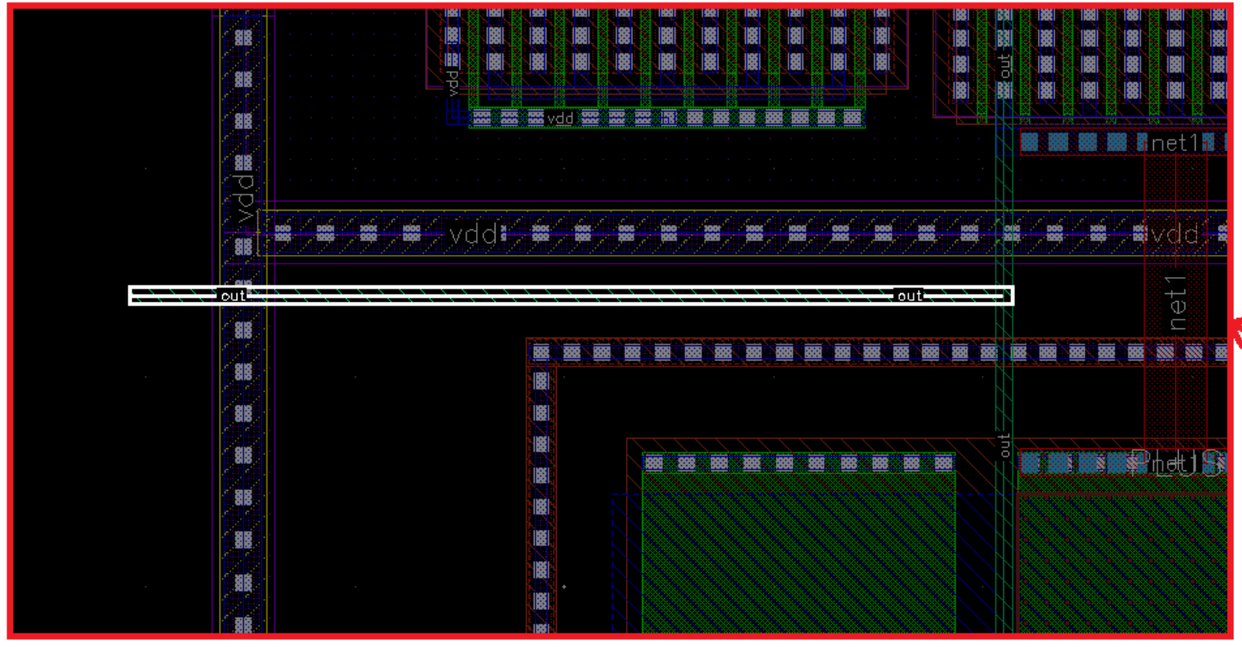
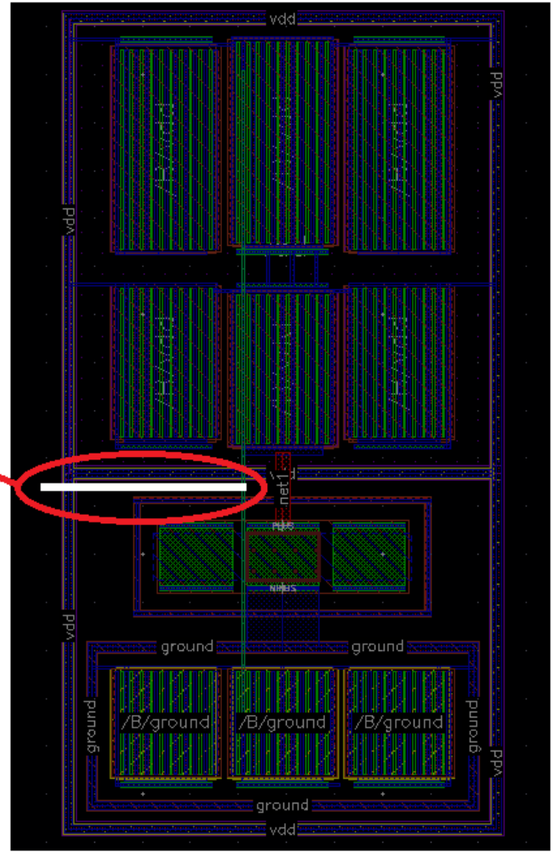
5. Routing the Components *(continued)*

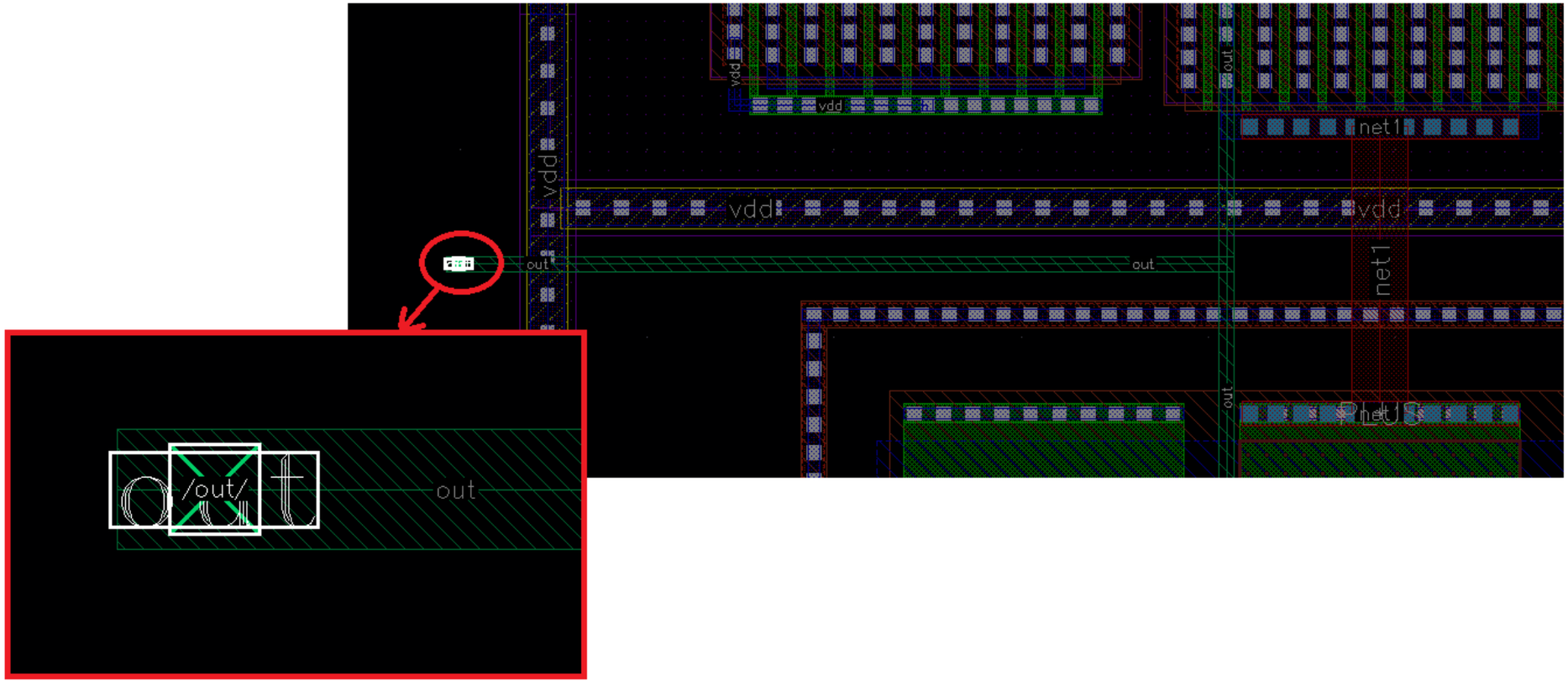
- Create a Metal3 path as shown in the figure below.





5. Routing the Components *(continued)*

- From the toolbar, change the Edit/Snap mode to Any Angle  .
- Select both the pin and the label **out** and place them both on the Metal3 layer as shown below.



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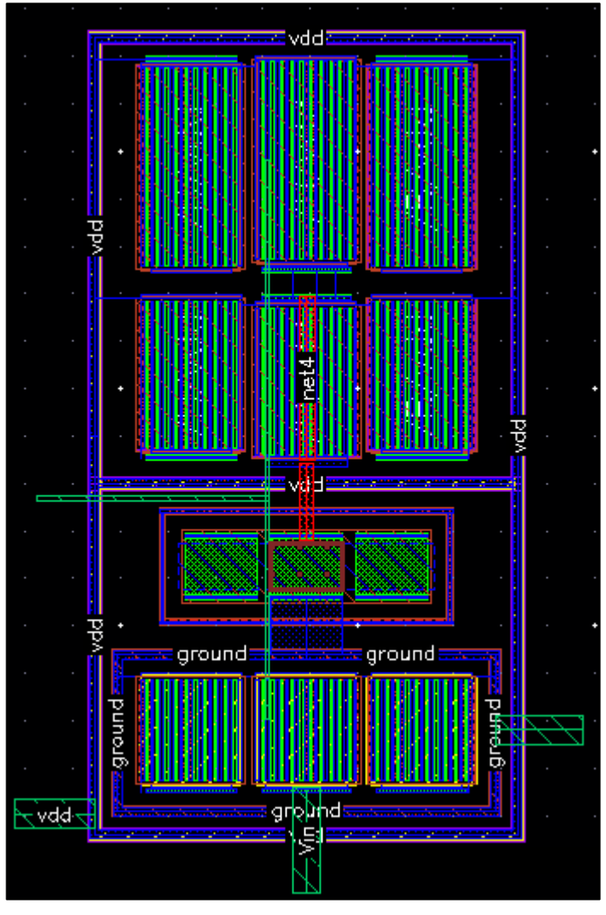
5. Routing the Components *(continued)*

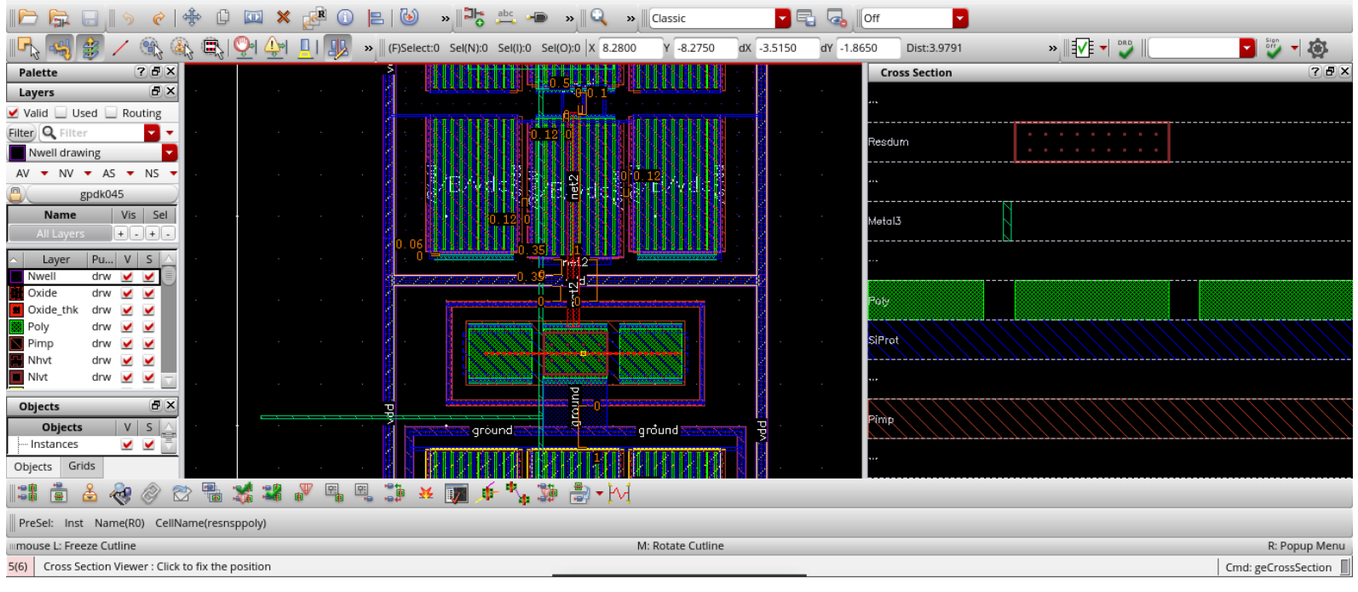
- The Vout and Vin labels are text layers, thus they are not part of the layout. The final layout is shown below.



- Note that a layout can always be improved.
- This layout might not be the best one, however, as a first attempt, it is quite good.

5. Routing the Components *(continued)*

- We can also view the cross-section of the layout by clicking on Window => Assistants => Cross Section
- The viewer displays the different layers present in a cross-section, from top to bottom. This is helpful when you want to identify any missing or wrongly placed layers or debug any connection issues across layers.
- When you invoke Cross Section Viewer, a cutline appears on the canvas that follows the pointer. As you hover the cutline over the design, the cross-section of the area underneath the cutline is displayed in the viewer.



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