

Virtuoso 23.1

Module 9 – Physical Verification

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Contents

1. Design Rule Check (DRC)
2. Layout Versus Schematic (LVS)

Module Objective

In this module, we will run the Physical Verification Systems, namely, the Design Rule Check (DRC) and the Layout Versus Schematic (LVS).

1. Design Rule Check (DRC)

Design Rule Check (DRC)

Layout Versus
Schematic
(LVS)

1. Design Rule Check (DRC)

- First, we will run DRC. It will check every polygon, path, and rectangle in the design against strict rules and report violations. The rules are documented by Cadence, and the document can be found in the folder “docs” of the pdk.
- The rules consist of spacing between layers, minimum dimensions, enclosed area, placements on the grid...
- Open the **layout view** of the common source amplifier.
- From the toolbar, PVS → Run DRC. (If PVS does not appear in the toolbar, click Launch → Layout EXL)
- The DRC Run Submission Form opens.
- Enter the following for the Run Directory: **“amplifier_common_source/cs_amplifier/drc”**
- Note that the tool will automatically create the folder “drc” in the cs_amplifier folder.



Design Rule Check (DRC)

Layout Versus Schematic (LVS)

1. Design Rule Check (DRC) (continued)

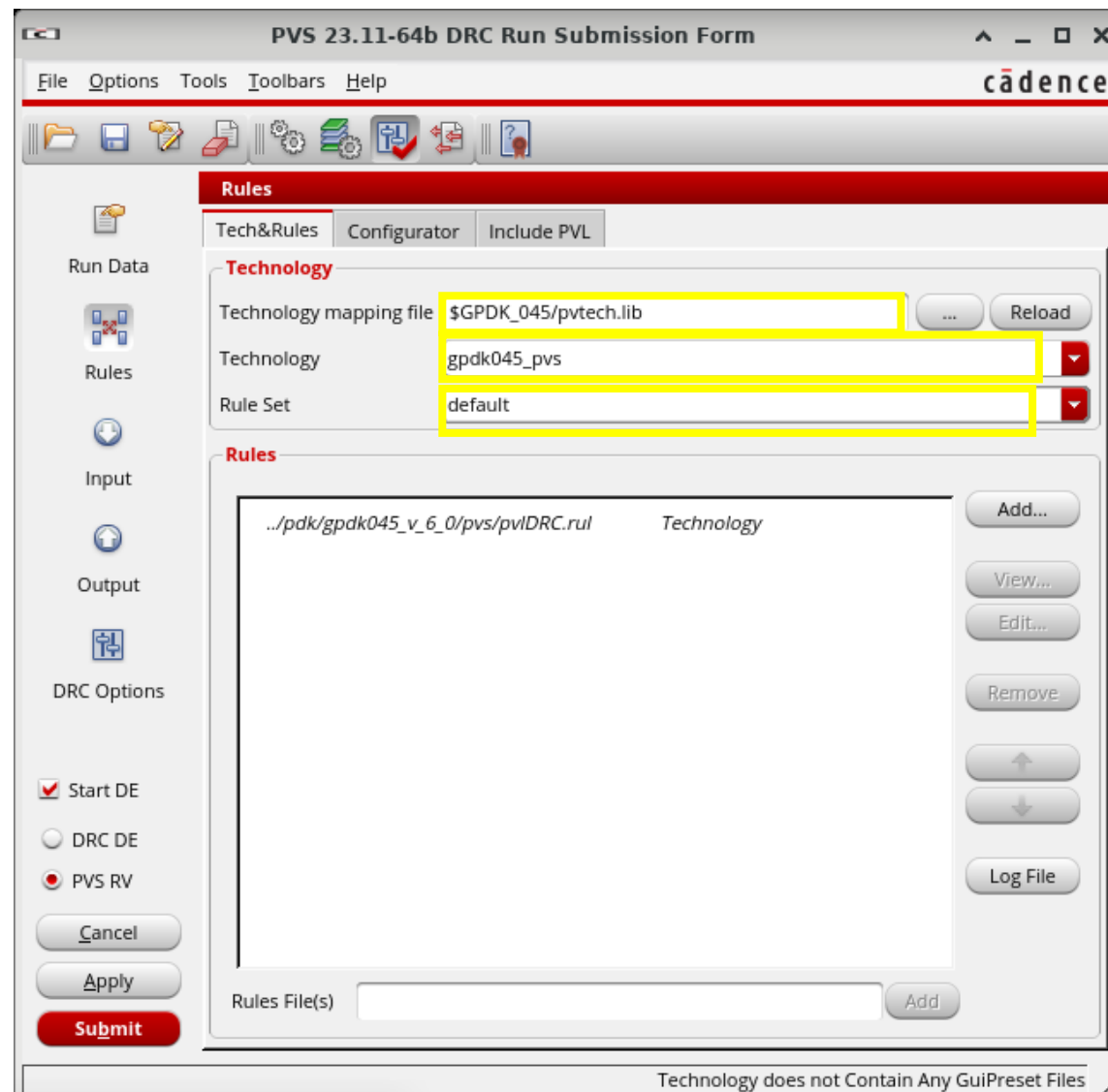
➤ Rules

- For the Technology mapping file, type the following:

“\$GPDK_045/pvtech.lib”

Note that “GPDK_045” must point to the root folder “gpdk045_v_6_0”.

- Set the Technology and Rule Set from the drop-down list to gpdk045_pvs and default, respectively.



- Note that the following is the whole path for the technology file:
“../pdk/gpdk045/gpdk045_v_6_0/pvtech.lib”

Design Rule
Check (DRC)

Layout Versus
Schematic
(LVS)

1. Design Rule Check (DRC) *(continued)*

- The **Input** parameters are set by default.



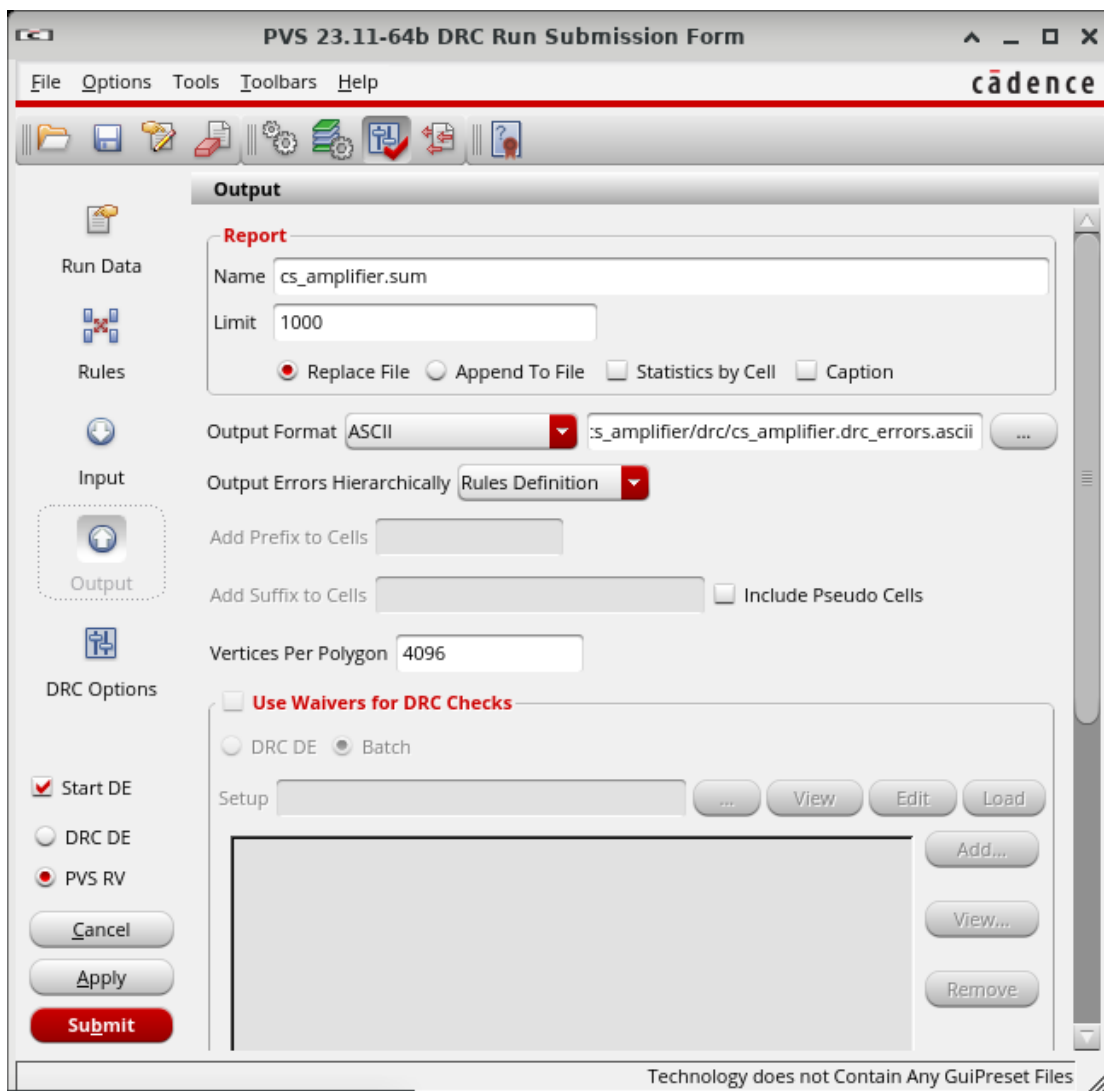
The screenshot shows the 'PVS 23.11-64b DRC Run Submission Form' window in Cadence. The 'Layout' tab is active, and the 'Input' section is highlighted. The 'Library' is set to 'amplifier_common_source', the 'Cell' is 'cs_amplifier', and the 'View' is 'layout'. The 'Create GDSII' checkbox is checked, and the file path is '/ifier_common_source/cs_amplifier/drc/cs_amplifier.gds'. The 'Layer Map List' shows a file path: '/home/user/pdk/gpdk045_v_6_0/gpdk045/gpdk045.lay'. The 'Cell Name Table', 'Object Name Table', and 'Label Map Table' are empty. The 'Convert Pin to' options are 'Geometry' (selected), 'Text', 'Geometry+Text', and 'Ignore'. The 'Start DE' checkbox is checked, and the 'DRC DE' and 'PVS RV' checkboxes are unchecked. The 'Hierarchy Depth Limit' is set to 32, and the 'Maximum Vertices In Path/Polygon' is set to 2048. The 'Enable Coloring' checkbox is checked. The 'Submit' button is highlighted in red.

Design Rule
Check (DRC)

Layout Versus
Schematic
(LVS)

1. Design Rule Check (DRC) *(continued)*

- The **Output** parameters are set by default.



The screenshot shows the 'PVS 23.11-64b DRC Run Submission Form' window. The 'Output' tab is selected in the left sidebar. The main area contains the following settings:

- Report:**
 - Name: cs_amplifier.sum
 - Limit: 1000
 - Buttons: ☒ Replace File, ☐ Append To File, ☐ Statistics by Cell, ☐ Caption
- Output Format:** ASCII (dropdown menu)
- Output Errors Hierarchically:** Rules Definition (dropdown menu)
- Add Prefix to Cells:** (empty text field)
- Add Suffix to Cells:** (empty text field) ☐ Include Pseudo Cells
- Vertices Per Polygon:** 4096
- DRC Options:**
 - ☒ Start DE
 - ☐ DRC DE
 - ☒ PVS RV
 - ☐ Use Waivers for DRC Checks
 - ☐ DRC DE ☒ Batch
 - Buttons: Setup, View, Edit, Load, Add..., View..., Remove

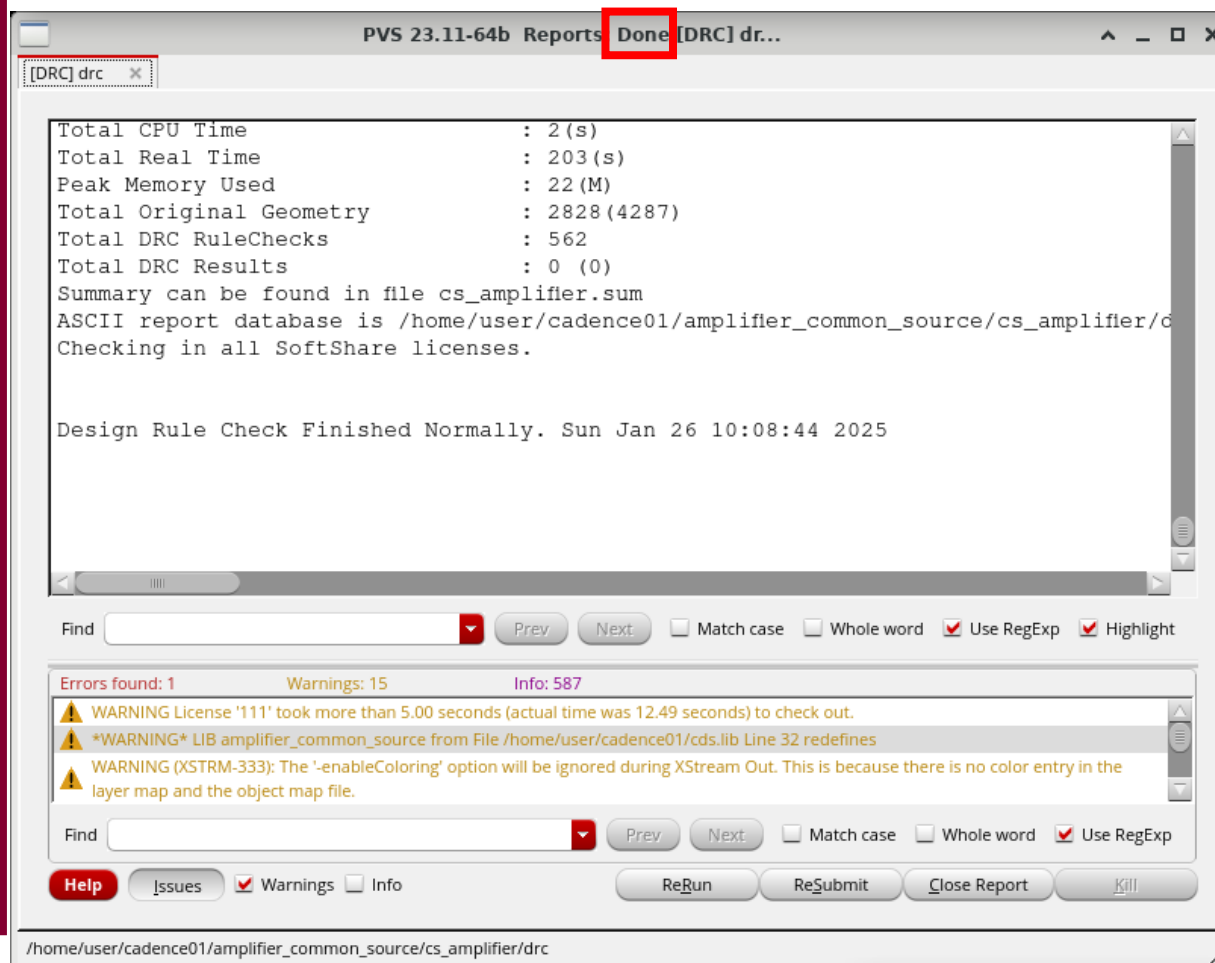
At the bottom, there are buttons for Cancel, Apply, and Submit. A footer note states: 'Technology does not Contain Any GuiPreset Files'.

Design Rule
Check (DRC)

Layout Versus
Schematic
(LVS)

1. Design Rule Check (DRC) *(continued)*

- Click **Submit** and the verification should be running.
- Wait for the report to say Done [DRC] at the top and wait a little bit for the Results Viewer window to pop up.



- In any of the verification systems, the errors will be clearly stated along with how to fix them.

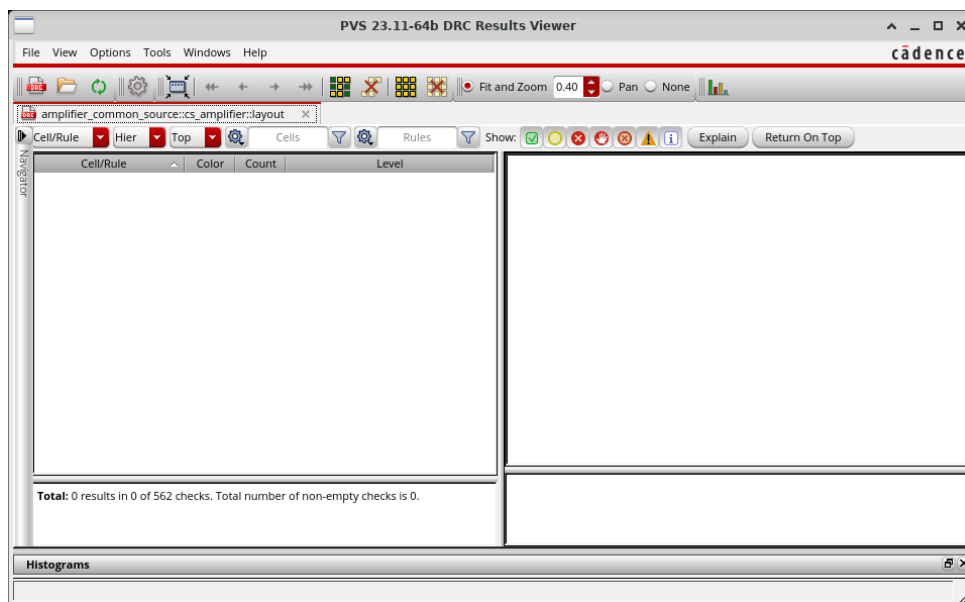
Design Rule
Check (DRC)

Layout Versus
Schematic
(LVS)

1. Design Rule Check (DRC) (*continued*)

- After a while, the Results Viewer window opens, and it will clearly indicate the errors if any. Click on an error and click Explain to highlight the error in the Layout.
- All the errors **must be fixed** before proceeding with the module.
- The full documentation of the rules can be found on the desktop “gpdK045v6_Docs/gpdK045_drc.pdf” or from “../pdk/gpdK045/gpdK045_v_6_0/docs/gpdK045_drc.pdf” (You can search for the error using Ctrl+F, and for further clarification make sure to check the figures related to the error).
- If the layout does not violate any of the rules, the Results Viewer window will be empty as shown below (close the results viewer before proceeding).

- In any of the verification systems, the errors will be clearly stated along with how to fix them.



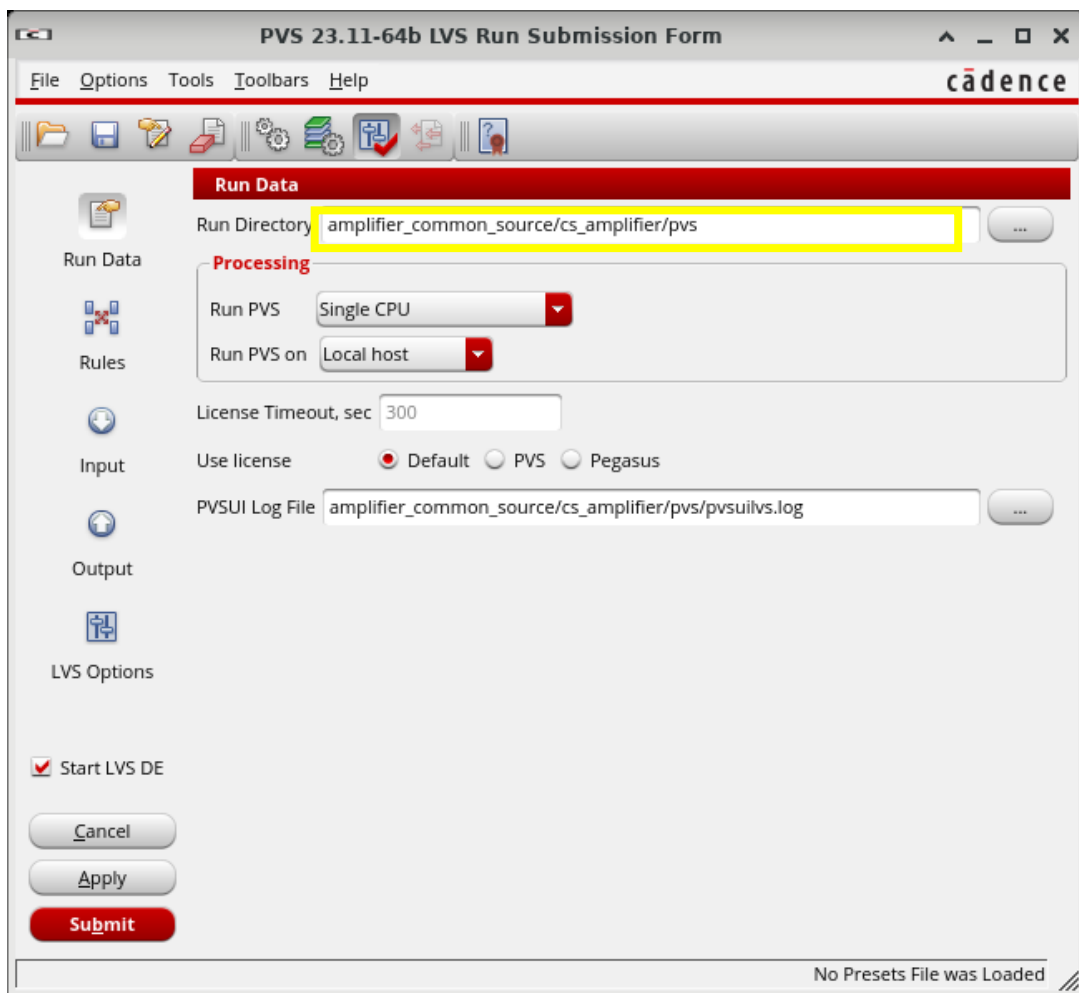
2. Layout Versus Schematic (LVS)

Design Rule
Check (DRC)

Layout Versus
Schematic
(LVS)

2. Layout Versus Schematic (LVS)

- From the toolbar, PVS → Run LVS.
- For the Run Directory, type: **“amplifier_common_source/cs_amplifier/pvs”**



PVS 23.11-64b LVS Run Submission Form

File Options Tools Toolbars Help

Run Data

Run Directory: amplifier_common_source/cs_amplifier/pvs

Processing

Run PVS: Single CPU

Run PVS on: Local host

License Timeout, sec: 300

Use license: ☒ Default ☐ PVS ☐ Pegasus

PVSUI Log File: amplifier_common_source/cs_amplifier/pvs/pvsuivls.log

☒ Start LVS DE

Cancel Apply Submit

No Presets File was Loaded

- LVS compares the layout with the schematic, and reports whether they correspond to each other or not.
- Note that the tool will automatically create the folder “pvs” in the cs_amplifier folder.

Design Rule
Check (DRC)

Layout Versus
Schematic
(LVS)

2. Layout Versus Schematic (LVS) *(continued)*

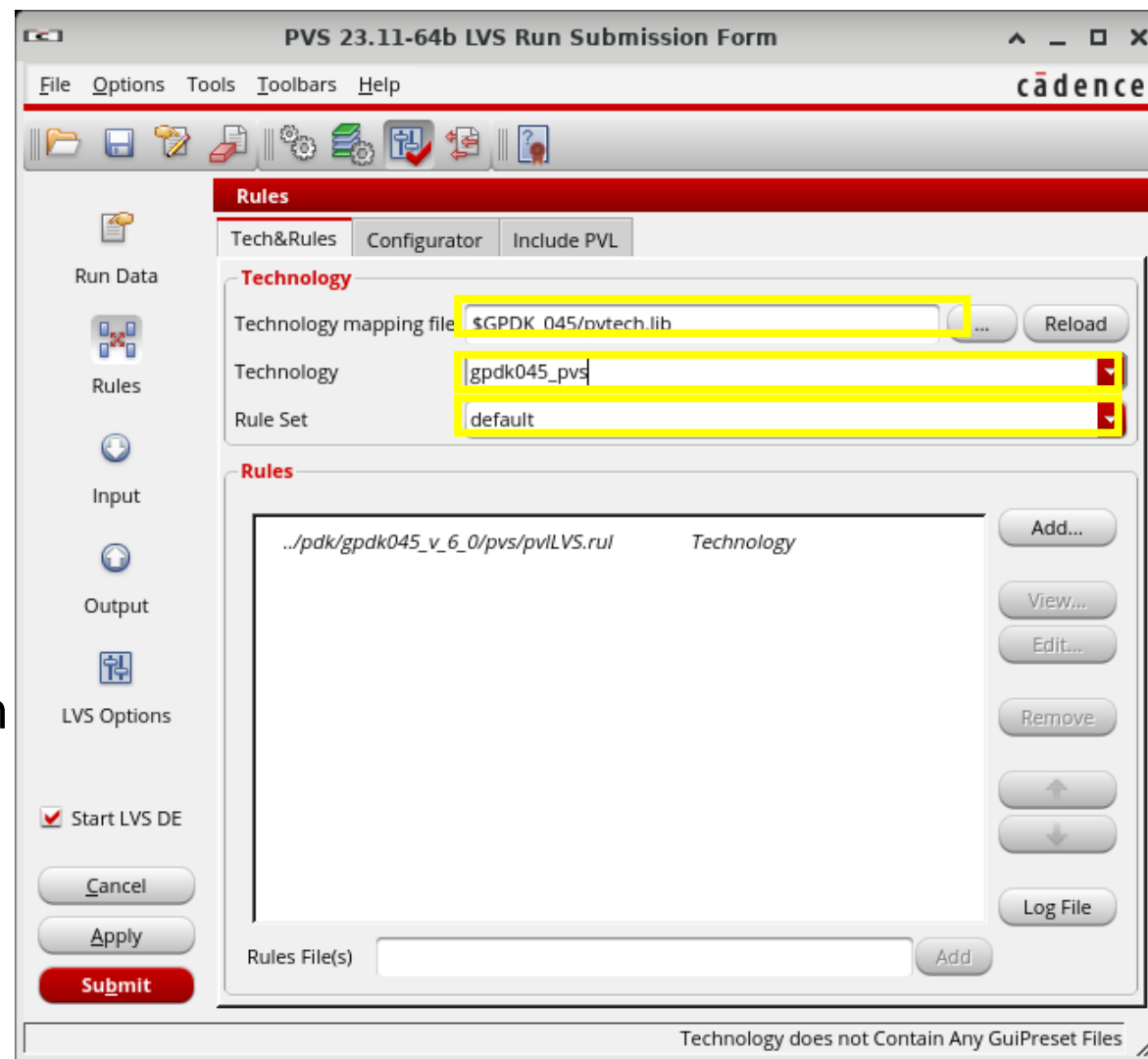
➤ Rules

- For the Technology mapping file, type the following:

“\$GPDK_045/pvtech.lib”

Note that “GPDK_045” must point to the root folder “gpdk045_v_6_0”.

- Set the Technology and Rule Set from the drop-down list to gpdk045_pvs and default, respectively.

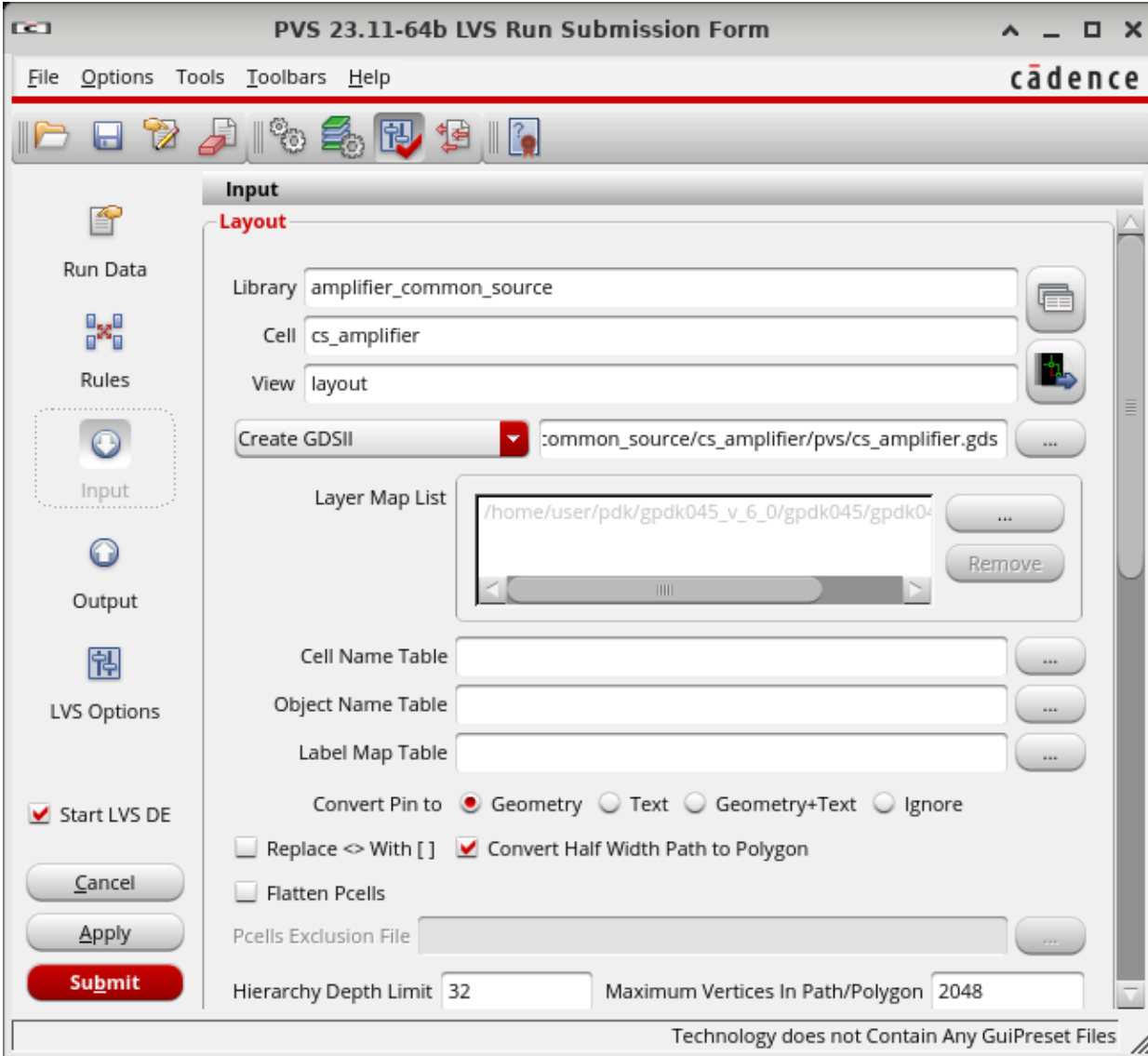


Design Rule
Check (DRC)

Layout Versus
Schematic
(LVS)

2. Layout Versus Schematic (LVS) *(continued)*

- The **Input** parameters are set by default.



PVS 23.11-64b LVS Run Submission Form

File Options Tools Toolbars Help

cadence

Input

Layout

Library: amplifier_common_source

Cell: cs_amplifier

View: layout

Create GDSII: ☒ :common_source/cs_amplifier/pvs/cs_amplifier.gds

Layer Map List: /home/user/pdk/gpdk045_v_6_0/gpdk045/gpdk045

Cell Name Table: ...

Object Name Table: ...

Label Map Table: ...

Convert Pin to: ☒ Geometry ☐ Text ☐ Geometry+Text ☐ Ignore

☐ Replace <-> With [] ☒ Convert Half Width Path to Polygon

☐ Flatten Pcells

Pcells Exclusion File: ...

Hierarchy Depth Limit: 32 Maximum Vertices In Path/Polygon: 2048

Technology does not Contain Any GuiPreset Files

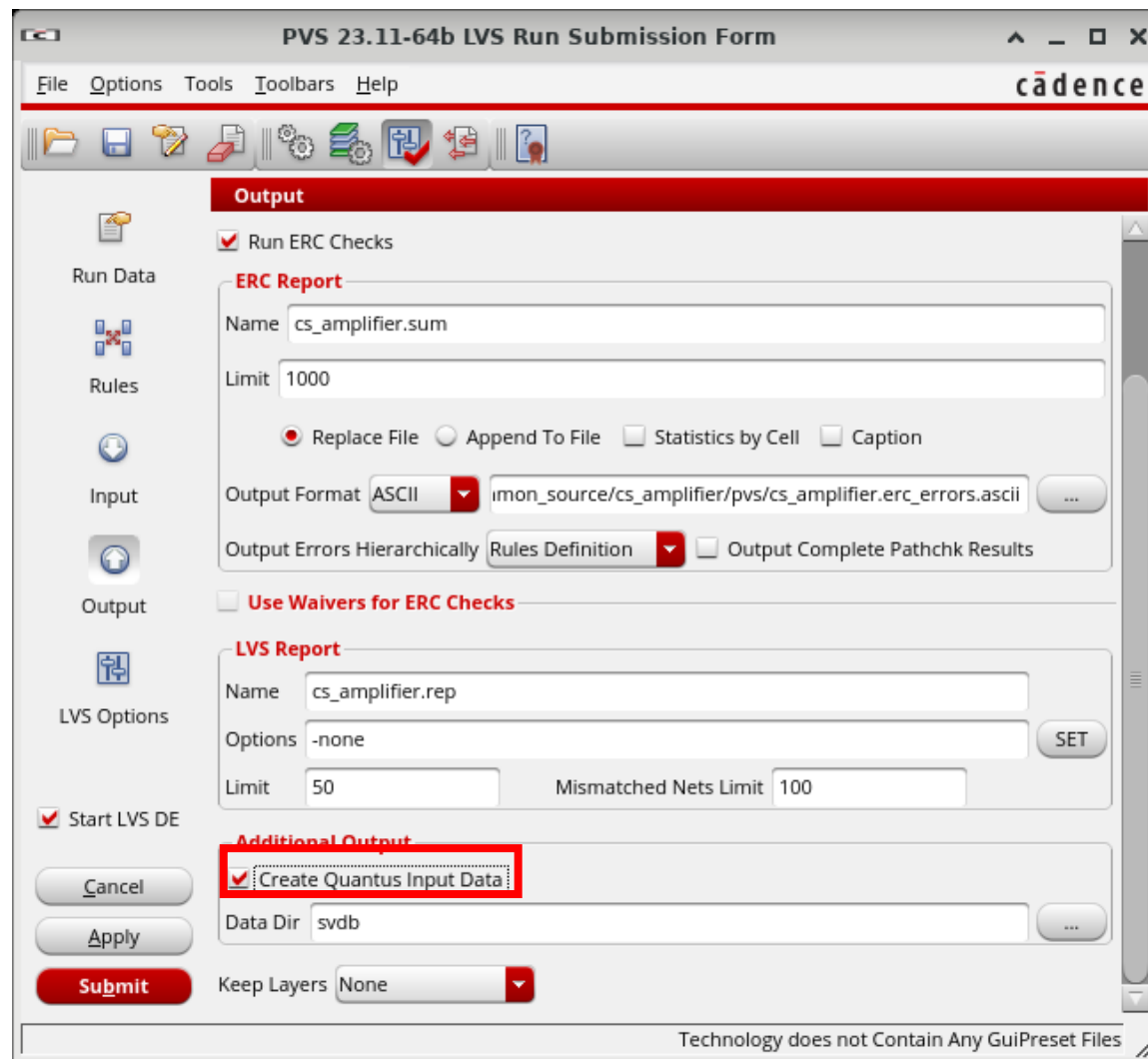
Cancel Apply Submit

Design Rule
Check (DRC)

Layout Versus
Schematic
(LVS)

2. Layout Versus Schematic (LVS) *(continued)*

- In the Output tab, make sure to check the checkbox **Create Quantus Input Data**.



The screenshot shows the 'PVS 23.11-64b LVS Run Submission Form' window. The 'Output' tab is selected in the left sidebar. The 'ERC Report' section has 'Name' set to 'cs_amplifier.sum', 'Limit' set to '1000', and 'Output Format' set to 'ASCII'. The 'LVS Report' section has 'Name' set to 'cs_amplifier.rep', 'Options' set to '-none', 'Limit' set to '50', and 'Mismatched Nets Limit' set to '100'. In the 'Additional Output' section, the checkbox 'Create Quantus Input Data' is checked and highlighted with a red box. The 'Data Dir' is set to 'svdb'. The 'Keep Layers' dropdown is set to 'None'. The 'Submit' button is highlighted in red.

- LVS and QRC are ran under the same directory.

Design Rule
Check (DRC)

Layout Versus
Schematic
(LVS)

2. Layout Versus Schematic (LVS) (continued)

- Click **Submit** and the verification should be running (it might take some time to finish).
- After a while, the LVS Run Status window pops-up. If the comparison has resulted in a mismatch, click Yes to view the errors.
- If the comparison results in a match, click Close to close the form.
- A match result means that the layout matches the schematic, i.e., the components, connections, component dimensions, etc., match the ones in the schematic.

- In any of the verification systems, the errors will be clearly stated along with how to fix them.

