AMERICAN UNIVERSITY OF BEIRUT

Virtuoso 23.1
Module 9 – Physical Verification

American University of Beirut (AUB)
Lebanon

cadence

© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

Contents

© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

Module Objective

In this module, we will run the Physical Verification Systems, namely, the Design Rule Check (DRC) and the Layout Versus Schematic (LVS).

© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

1. Design Rule Check (DRC)

© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

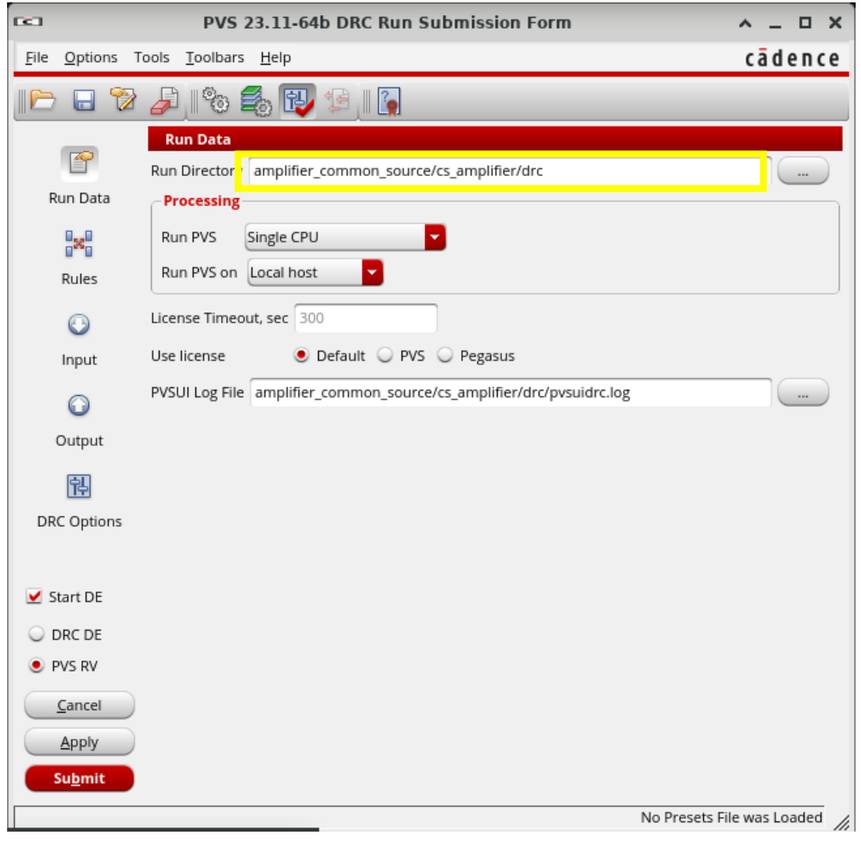
AMERICAN UNIVERSITY OF BEIRUT

Design Rule Check (DRC)

Layout Versus Schematic (LVS)

1. Design Rule Check (DRC)

- First, we will run DRC. It will check every polygon, path, and rectangle in the design against strict rules and report violations. The rules are documented by Cadence, and the document can be found in the folder “docs” of the pdk.
- The rules consist of spacing between layers, minimum dimensions, enclosed area, placements on the grid…
- Open the **layout view** of the common source amplifier.
- From the toolbar, PVS → Run DRC. (If PVS does not appear in the toolbar, click Launch → Layout EXL)
- The DRC Run Submission Form opens.
- Enter the following for the Run Directory: **“amplifier_common_source/cs_amplifier/drc”**
- Note that the tool will automatically create the folder “drc” in the cs_amplifier folder.



© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

cadence

AMERICAN UNIVERSITY OF BEIRUT

Design Rule Check (DRC)

Layout Versus Schematic (LVS)

1. Design Rule Check (DRC) *(continued)*

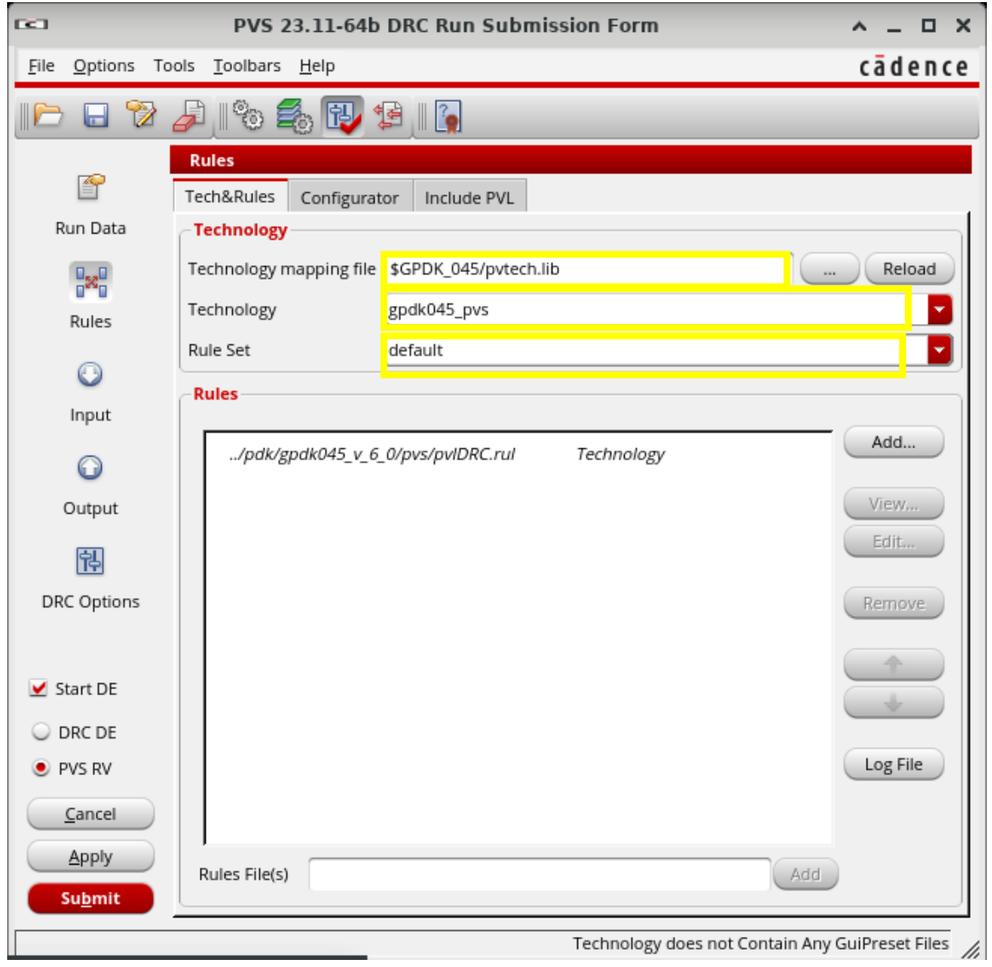
➢ Rules

- For the Technology mapping file, type the following:

  "$GPDK_045/pvtech.lib"

  Note that "GPDK_045" must point to the root folder "gpdk045_v_6 _0".

- Set the Technology and Rule Set from the drop-down list to gpdk045_pvs and default, respectively.



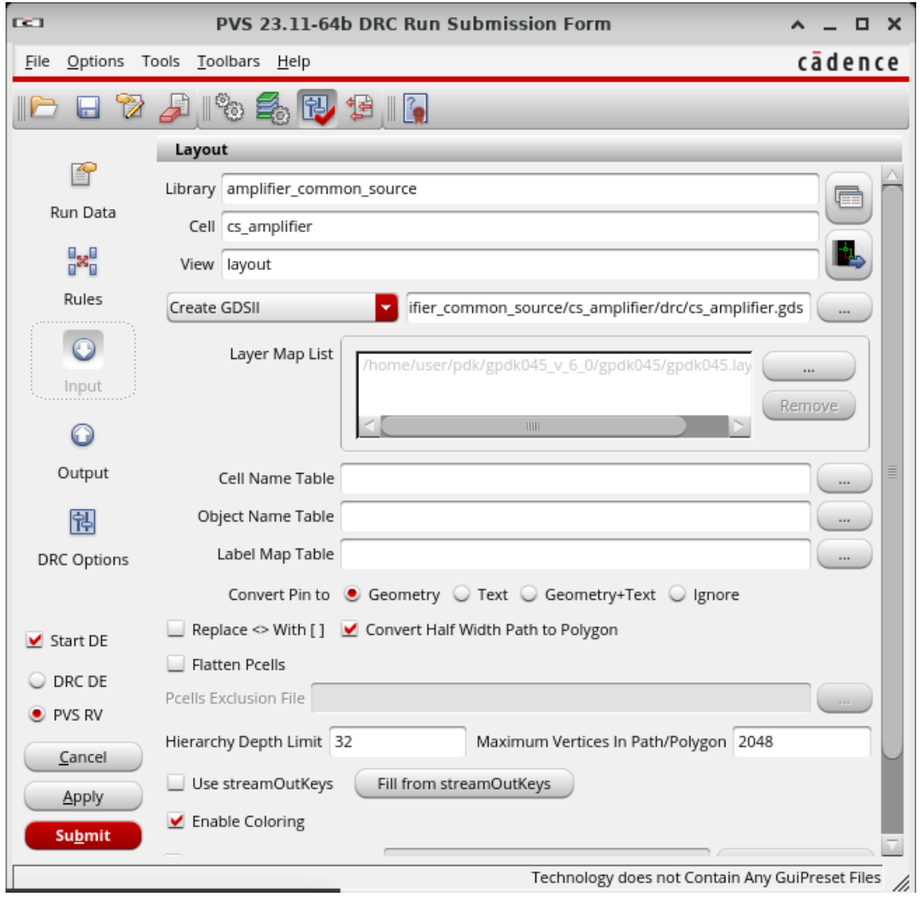
- Note that the following is the whole path for the technology file: "../pdk/gpdk045/gpdk045_v_6_0/pvtech.lib"

© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

cadence

1. Design Rule Check (DRC) *(continued)*

- The **Input** parameters are set by default.

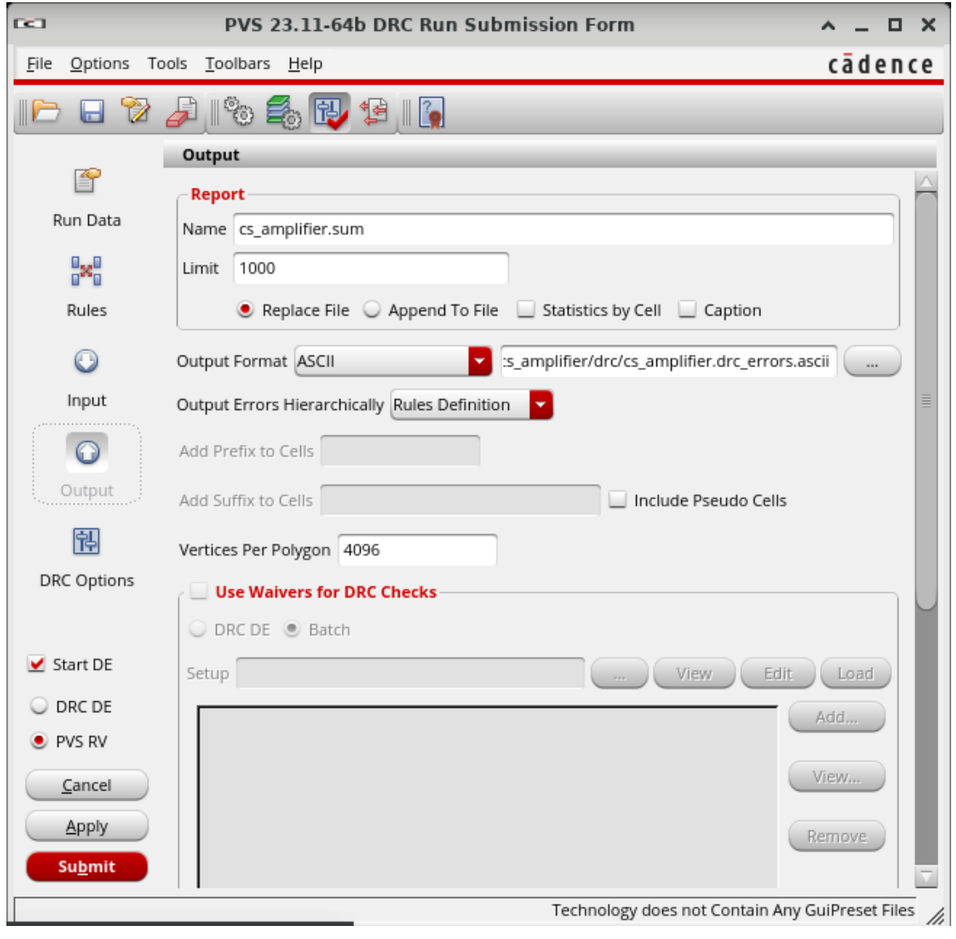


© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

cadence

1. Design Rule Check (DRC) *(continued)*

- The **Output** parameters are set by default.



© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

cadence

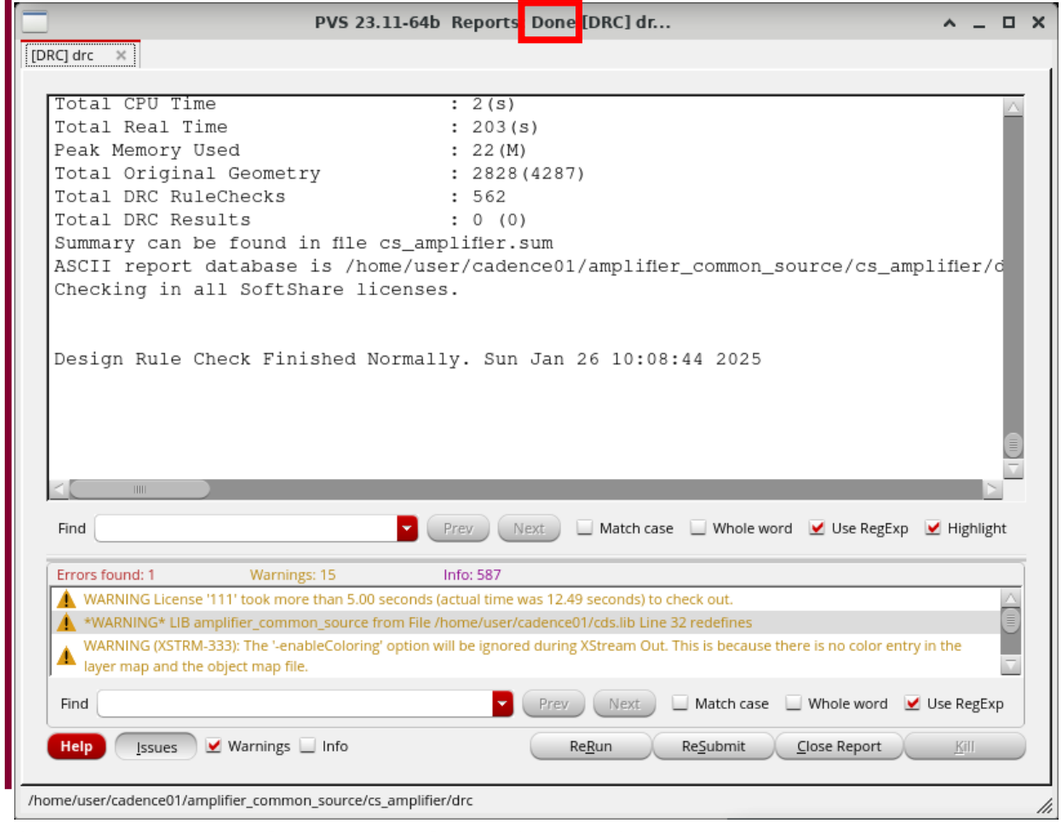
AMERICAN UNIVERSITY OF BEIRUT

Design Rule Check (DRC)

Layout Versus Schematic (LVS)

1. Design Rule Check (DRC) *(continued)*

- Click **Submit** and the verification should be running.
- Wait for the report to say Done [DRC] at the top and wait a little bit for the Results Viewer window to pop up.



- In any of the verification systems, the errors will be clearly stated along with how to fix them.

© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

cadence

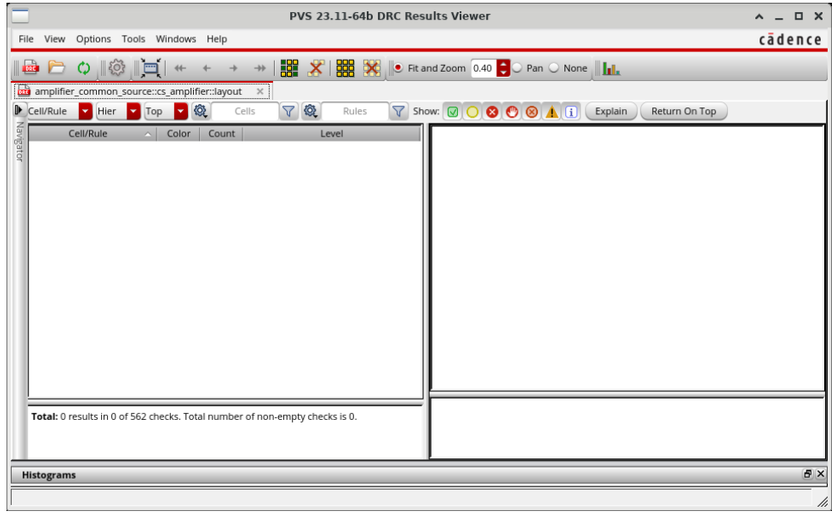
AMERICAN UNIVERSITY OF BEIRUT

Design Rule Check (DRC)

Layout Versus Schematic (LVS)

1. Design Rule Check (DRC) *(continued)*

- After a while, the Results Viewer window opens, and it will clearly indicate the errors if any. Click on an error and click Explain to highlight the error in the Layout.
- All the errors **must be fixed** before proceeding with the module.
- The full documentation of the rules can be found on the desktop "gpdk045v6_Docs/gpdk045_drc.pdf" or from "../pdk/gpdk045/gpdk045_v_6_0/docs/gpdk045_drc.pdf" (You can search for the error using Ctrl+F, and for further clarification make sure to check the figures related to the error).
- If the layout does not violate any of the rules, the Results Viewer window will be empty as shown below (close the results viewer before proceeding).



- In any of the verification systems, the errors will be clearly stated along with how to fix them.

© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

cadence

AMERICAN UNIVERSITY OF BEIRUT

2. Layout Versus Schematic (LVS)

© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

cadence

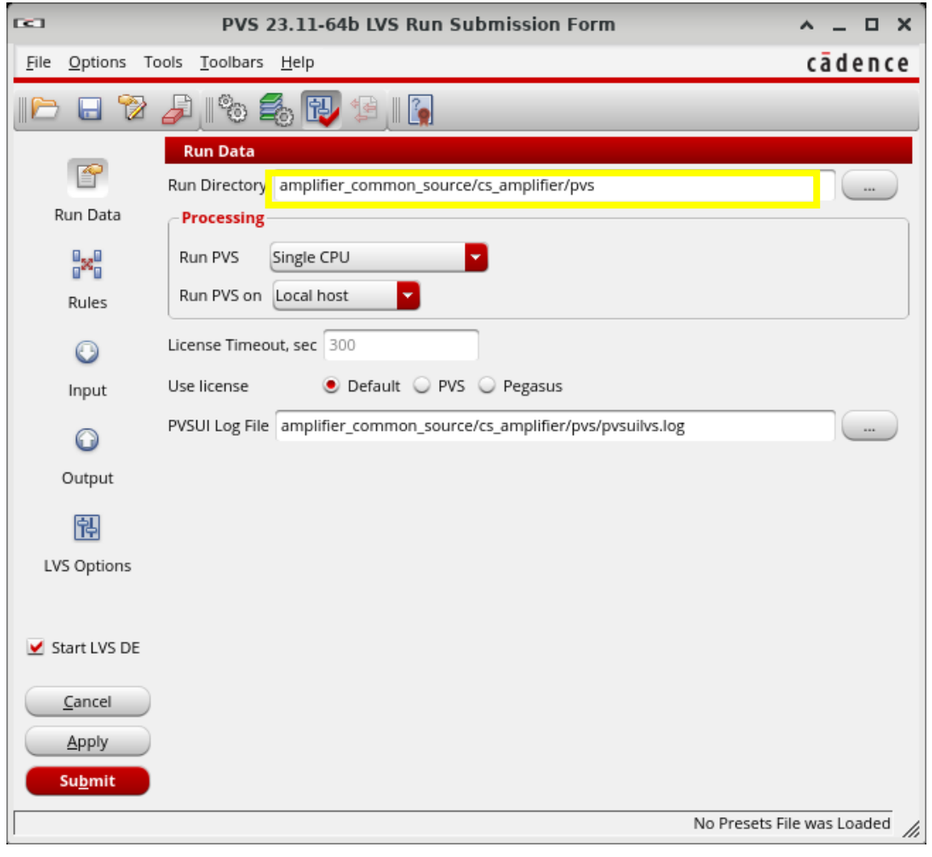
AMERICAN UNIVERSITY OF BEIRUT

Design Rule Check (DRC)

Layout Versus Schematic (LVS)

2. Layout Versus Schematic (LVS)

- From the toolbar, PVS → Run LVS.
- For the Run Directory, type: **“amplifier_common_source/cs_amplifier/pvs”**



- LVS compares the layout with the schematic, and reports whether they correspond to each other or not.
- Note that the tool will automatically create the folder “pvs” in the cs_amplifier folder.

cadence

© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

AMERICAN UNIVERSITY OF BEIRUT

Design Rule Check (DRC)

Layout Versus Schematic (LVS)

2. Layout Versus Schematic (LVS) *(continued)*

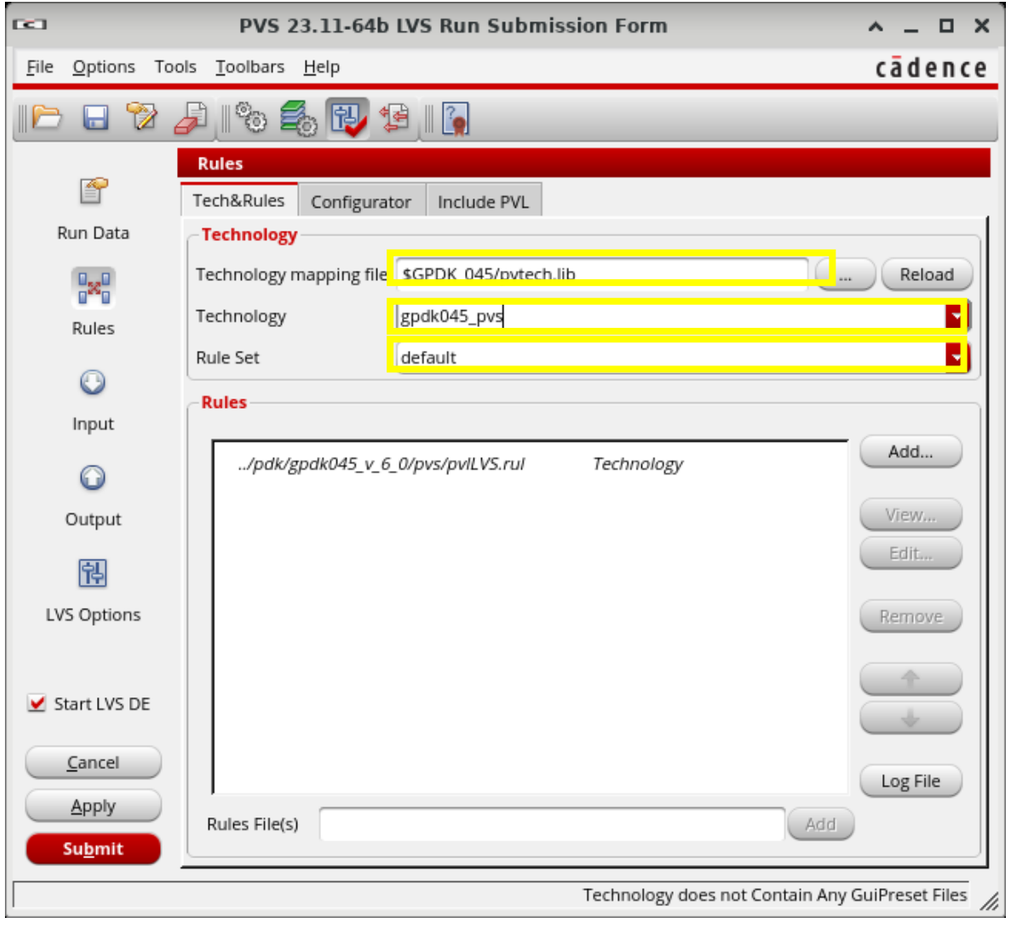
➢ Rules

- For the Technology mapping file, type the following:

  "$GPDK_045/pvtech.lib"

Note that "GPDK_045" must point to the root folder "gpdk045_v_6 _0".

- Set the Technology and Rule Set from the drop-down list to gpdk045_pvs and default, respectively.



© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

cadence

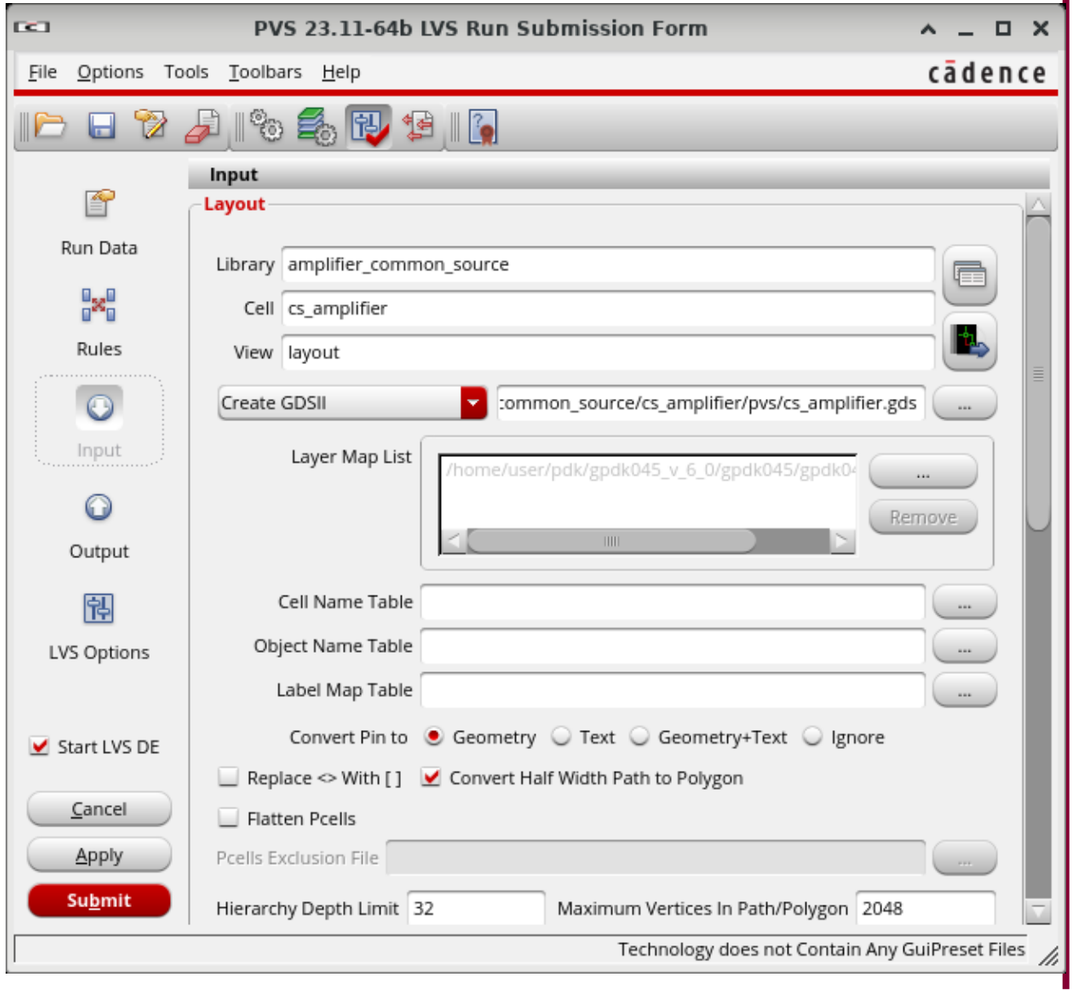
AMERICAN UNIVERSITY OF BEIRUT

Design Rule Check (DRC)

Layout Versus Schematic (LVS)

2. Layout Versus Schematic (LVS) *(continued)*

- The **Input** parameters are set by default.



© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

cadence

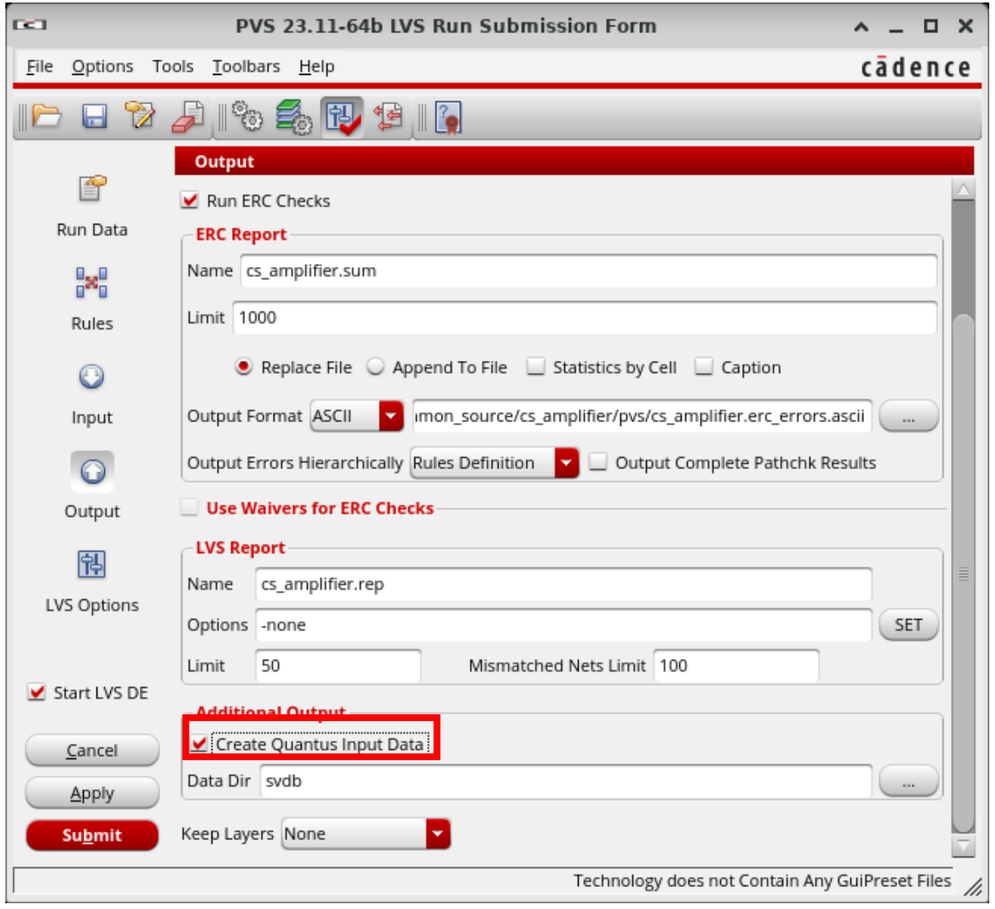
AMERICAN UNIVERSITY OF BEIRUT

Design Rule Check (DRC)

Layout Versus Schematic (LVS)

2. Layout Versus Schematic (LVS) *(continued)*

- In the Output tab, make sure to check the checkbox **Create Quantus Input Data**.



- LVS and QRC are ran under the same directory.

© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

cadence

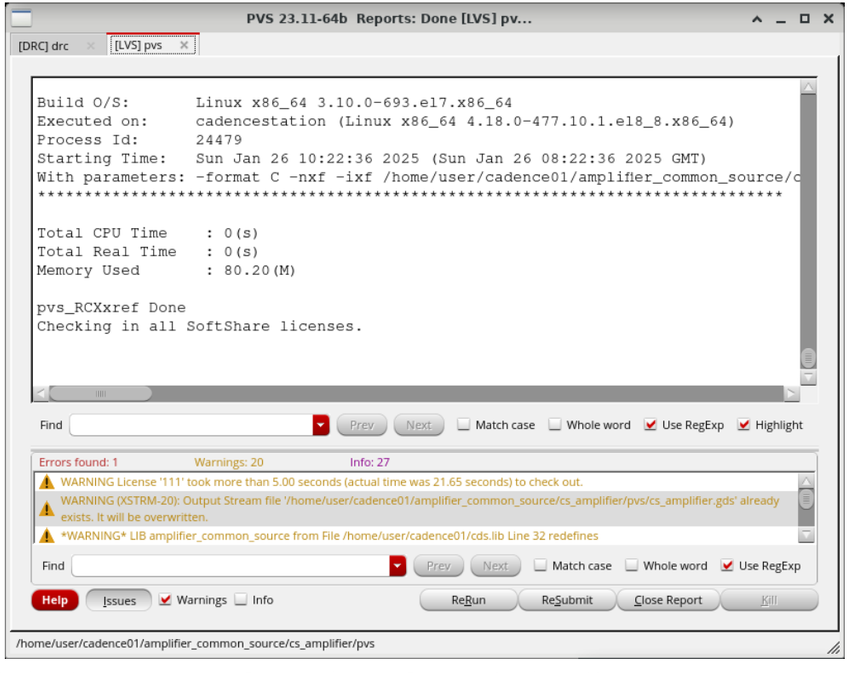
AMERICAN UNIVERSITY OF BEIRUT

Design Rule Check (DRC)

Layout Versus Schematic (LVS)

2. Layout Versus Schematic (LVS) *(continued)*

- Click **Submit** and the verification should be running (it might take some time to finish).
- After a while, the LVS Run Status window pops-up. If the comparison has resulted in a mismatch, click Yes to view the errors.
- If the comparison results in a match, click Close to close the form.
- A match result means that the layout matches the schematic, i.e., the components, connections, component dimensions, etc., match the ones in the schematic.



- In any of the verification systems, the errors will be clearly stated along with how to fix them.

© 2025 Jad Atallah. All rights reserved. Supported by the Cadence Academic Network.

cadence