

Virtuoso 23.1

Module 10 – EMIR analysis (Electromigration and IR drop)

American University of Beirut (AUB)
Lebanon

Contents

1. Introduction to EMIR and theoretical background
2. Setting up the EAD for Simulation
 - a) Activating the EAD Mode
 - b) Signal Selection to Save Current
 - c) Creating Datasets
3. Performing Electromigration Analysis
 - a) Setting up EAD Browser
 - b) Extracting Parasitics and Running EM Check
4. Fixing Violations

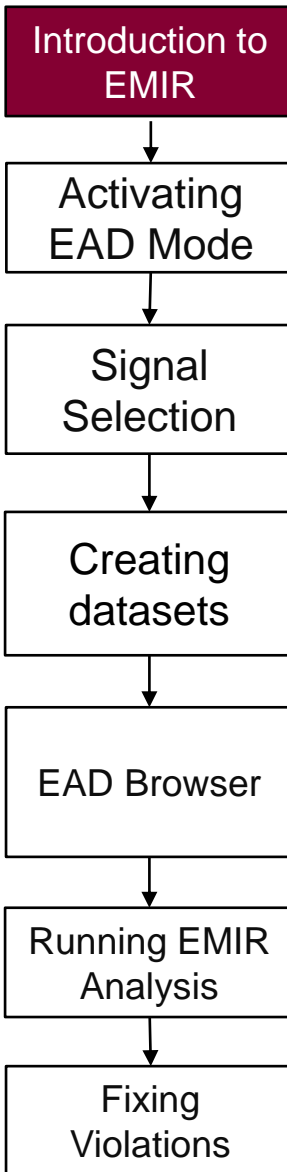
Module Objective

In this module, we will learn how to:

- Set up EAD mode in ADE Assembler
- Create Datasets by selecting signals from our schematic
- Use the Datasets created to perform EMIR analysis
- Optimizing the Layout to reduce EM violations

1. Introduction to Reliability and Theoretical Background

1. Introduction to EMIR and Theoretical Background



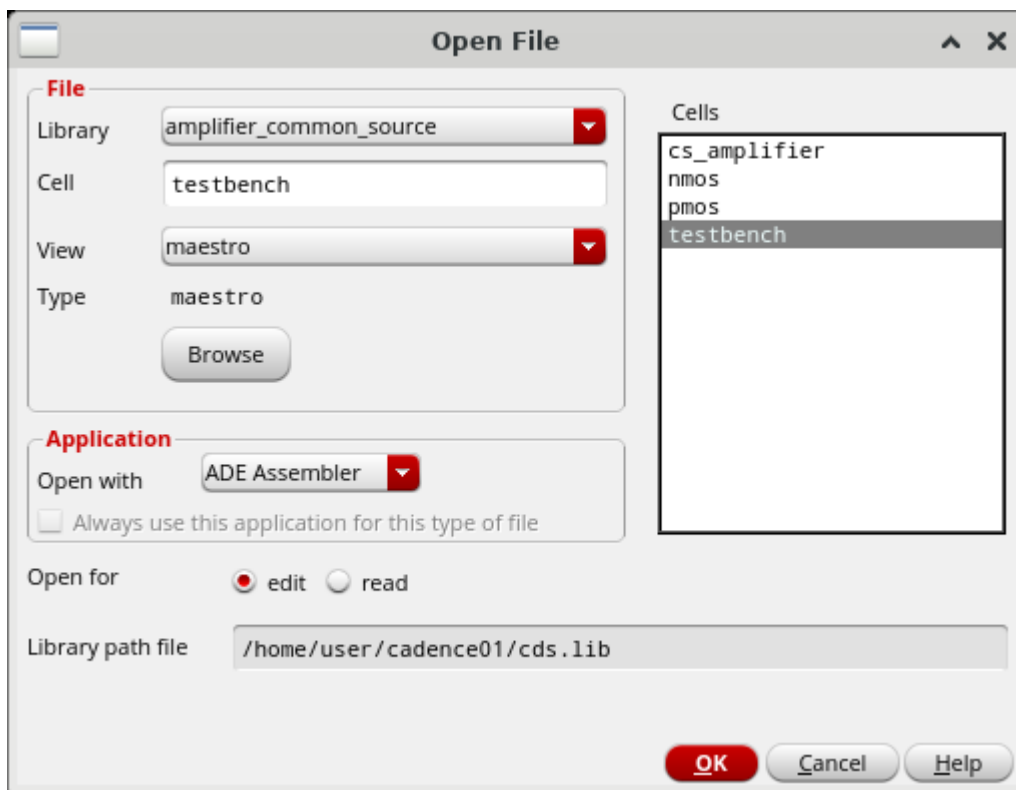
- EMIR (Electromigration and IR Drop) is one of the most challenging fields of circuit simulation. It consists of the Electromigration and IR Drop where both play a big role in the reliability of the design.
- Electromigration (EM) is a phenomenon that describes the displacement of atoms/ions in a solid conductor from their lattice points due to the collisions caused by the momentum transfer from the flow of electrons and the metal atoms in connecting wires.
- It is related to the current density: the higher the current density, the higher the risk of EM.
- The collisions caused by the movement of electrons cause the wires to become heated, which can lead to an open circuit, or a short metal wire if enough atoms move to the same spot.
- IR Drop is the voltage drop that occurs when current flows through a conductor with resistance. In PCBs and integrated circuits, IR drop is extremely important and can have negative effects, such as the destination voltage being somewhat lower than the source voltage.

- Note that EM takes years to happen (Gradually)

2. Setting up the EAD for Simulation

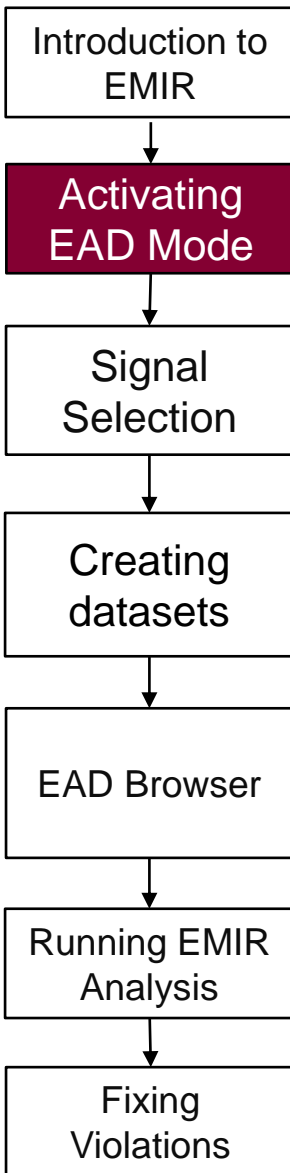
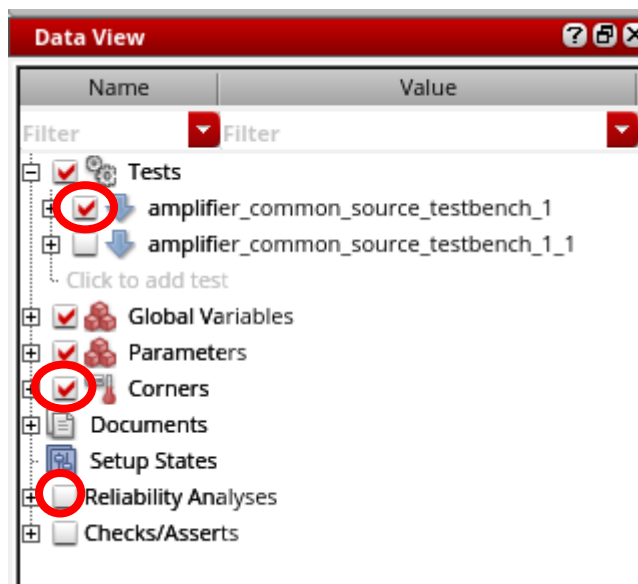
2.a) Activating The EAD Mode

- Select the “amplifier_common_source” library and highlight the testbench cell view then click on maestro view.
- The maestro view should be opened with ADE Assembler.



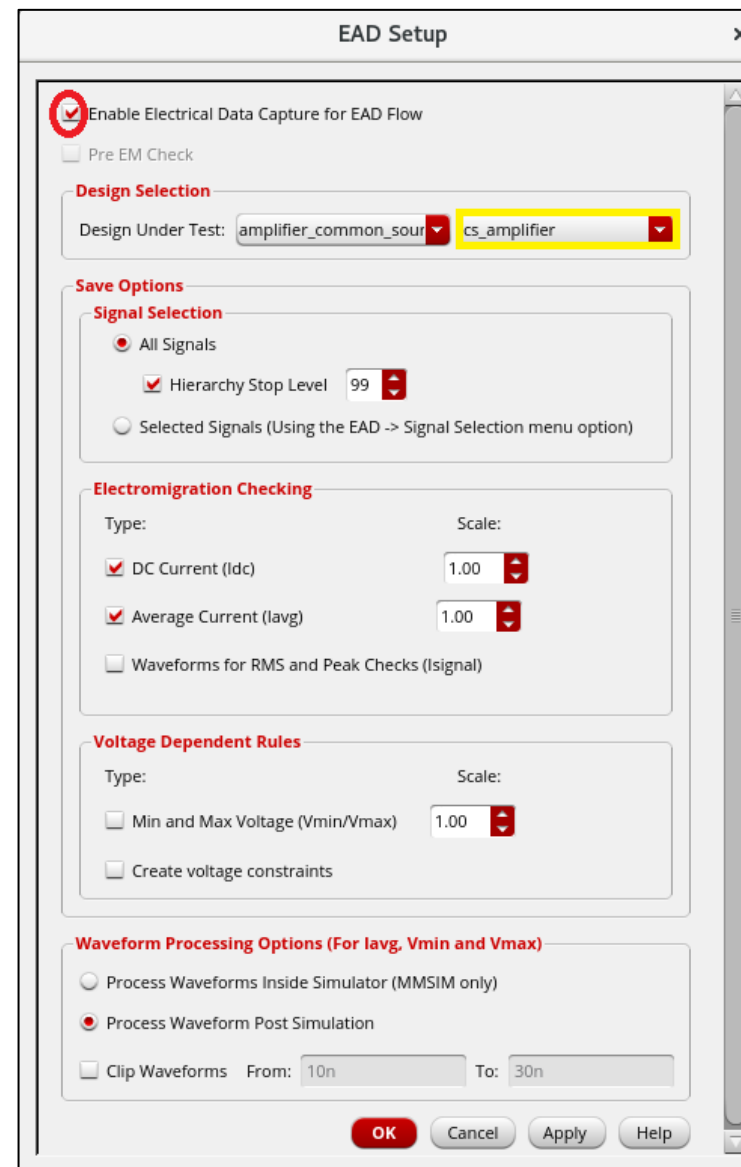
2.a) Activating The EAD Mode (Continued)

- In the Data view panel, make sure to select “amplifier_common_source_testbench_1” under tests, enable **corners** and disable **Reliability Analyses**. like the figure below.



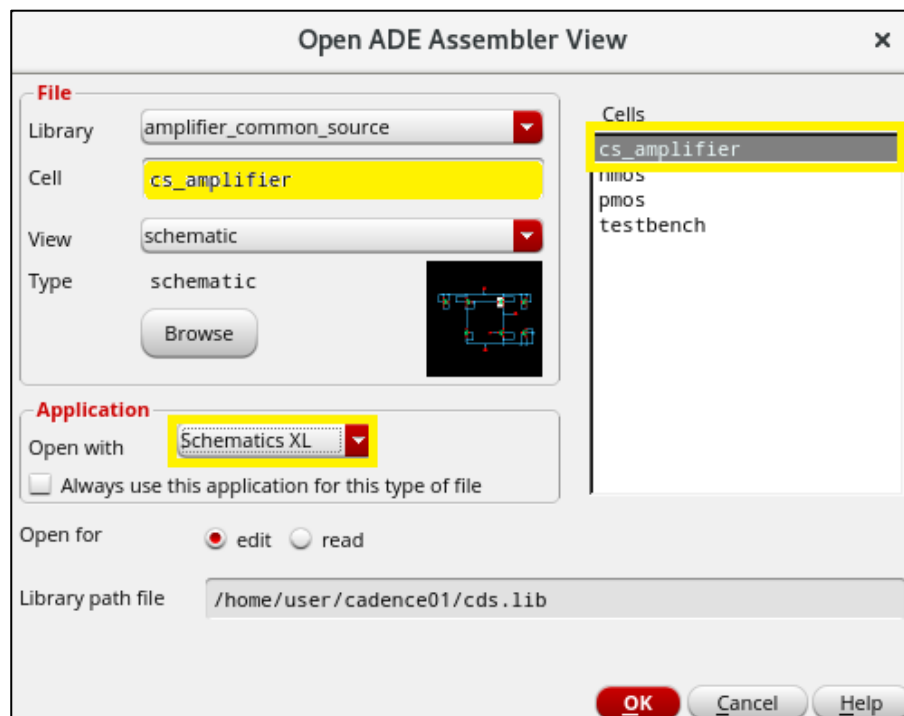
2.a) Activating The EAD Mode (Continued)

- Click on **EAD** from the upper tabs, then **Setup...**
- The EAD Setup browser will open.
- Enable Electrical Data Capture For EAD Flow.
- Under Design Selection, select **cs_amplifier** as a design.
- Click on **OK** to close the browser.



2.b) Signal Selection To Save Current

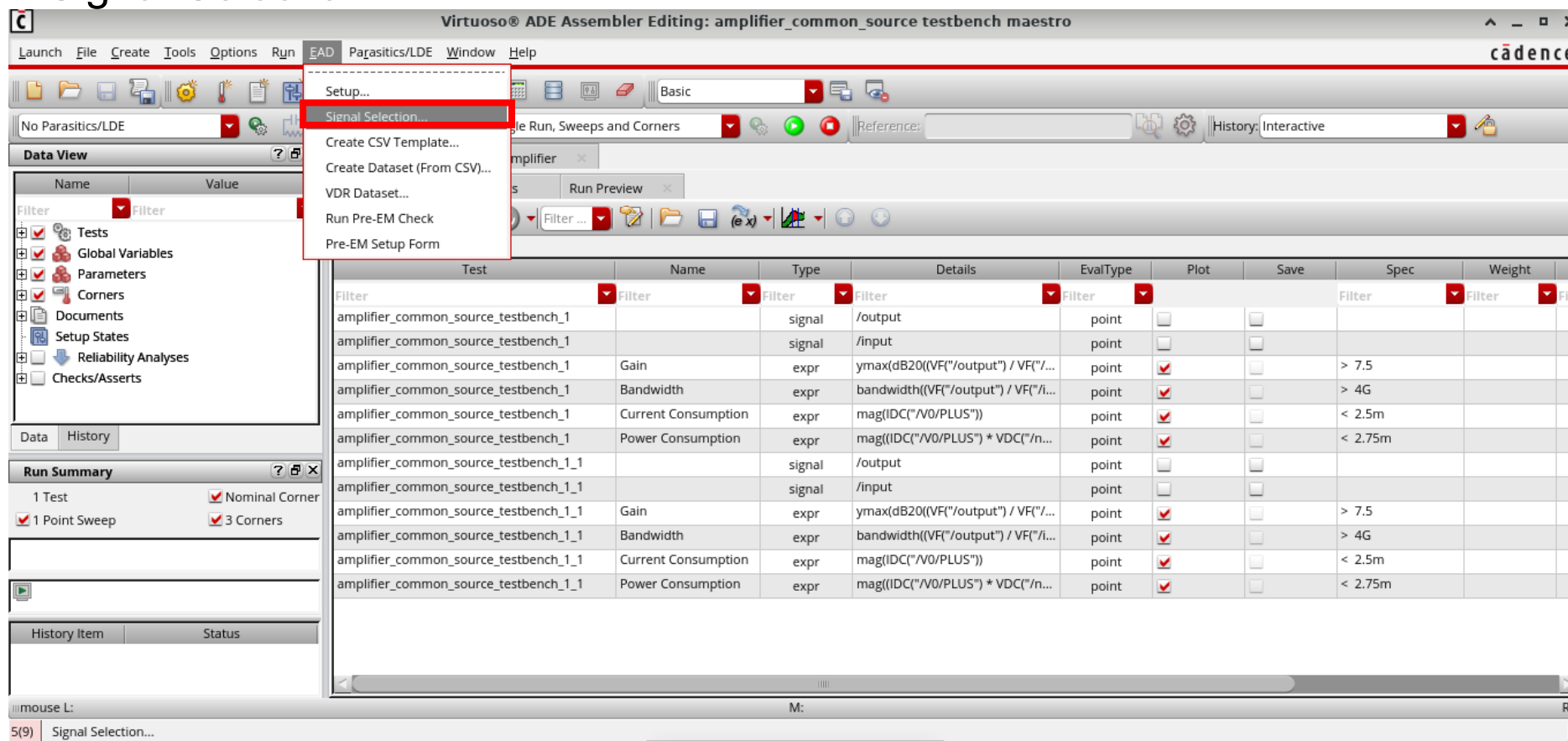
- From the upper tabs, click on **File -> Open...**
- Select the **amplifier_common_source** library, and the **cs_amplifier** cell.
- Next to view, select **Schematic**.
- Under Application, make sure to open with **Schematics XL**.



2.b) Signal Selection To Save Current (Continued)

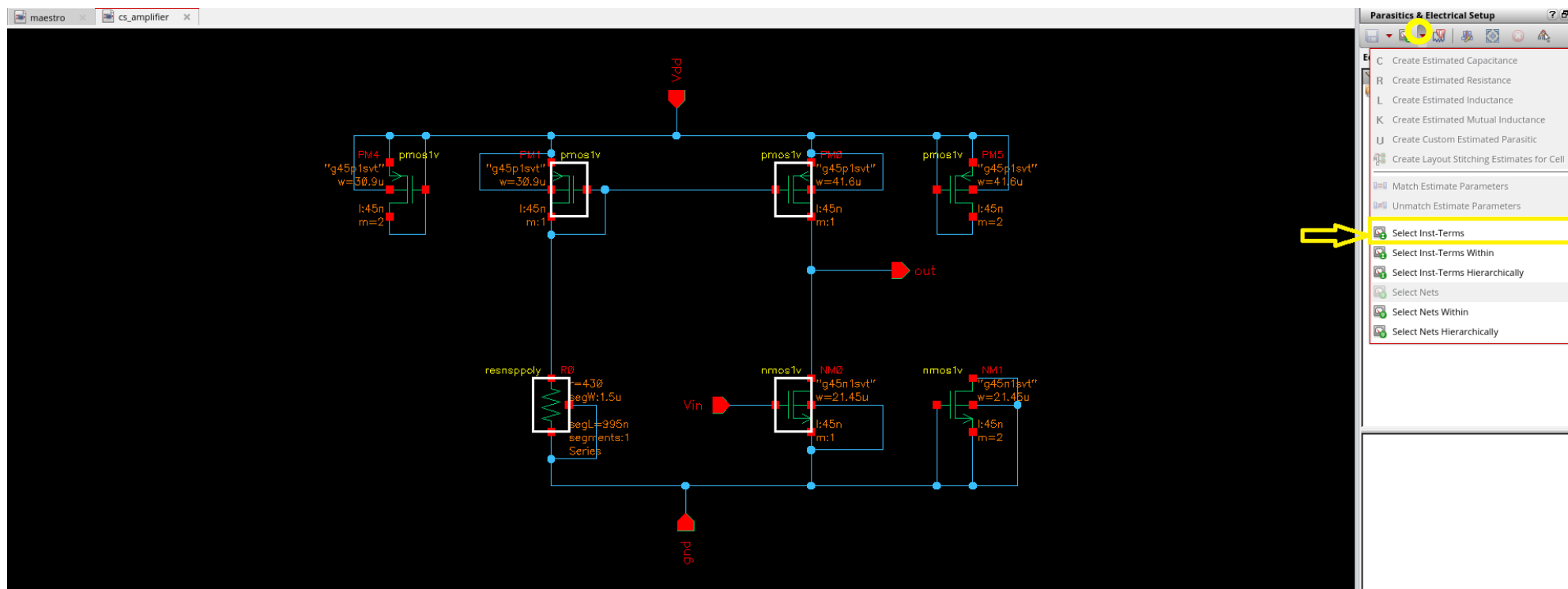
- Schematics XL will open, and this is where we select the currents for the Datasets.
- To select the signals, go back to the **maestro** view and From the tabs, click on EAD → Signal Selection...

- Note that Select Inst-Terms will select all the device's terminals.



2.b) Signal Selection To Save Current (Continued)

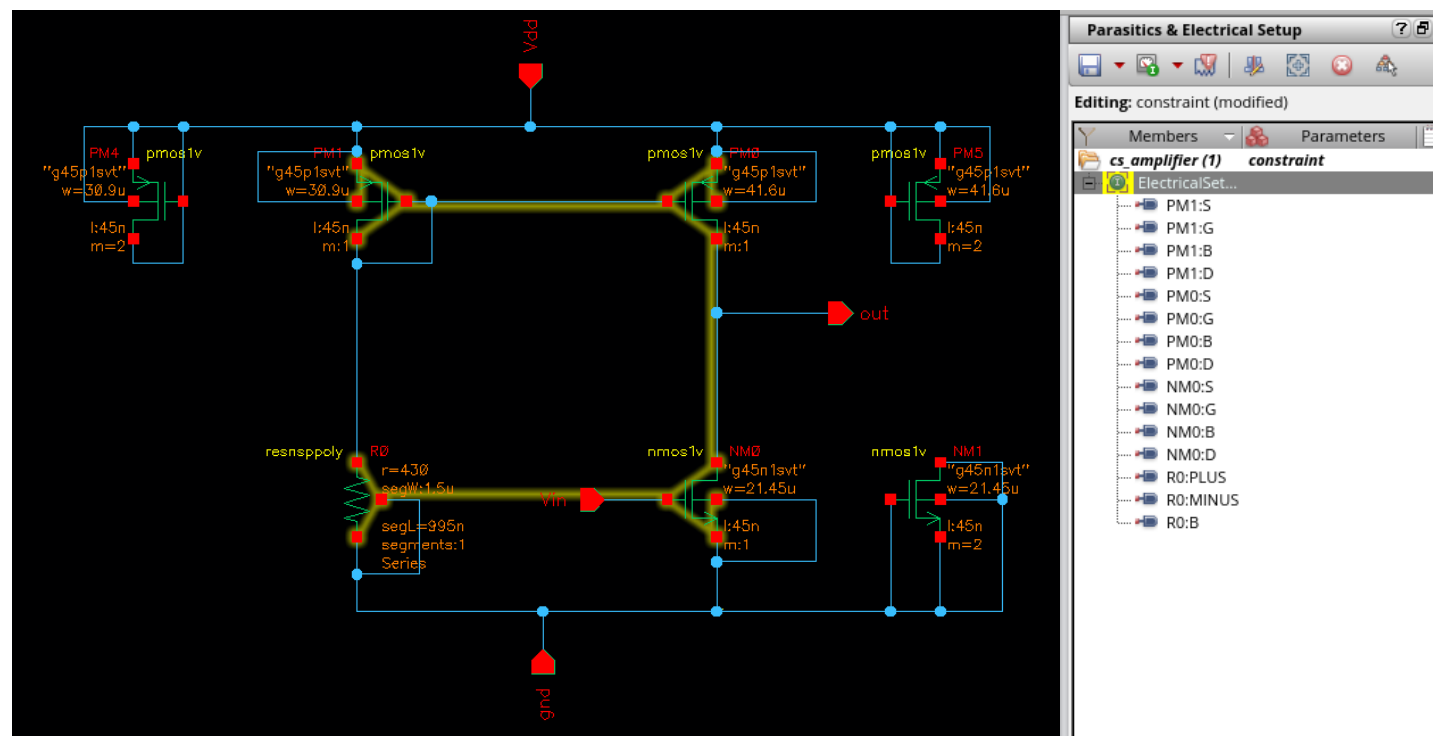
- Schematics XL will re-open with the **Parasitics & Electrical Setup** workspace.
- **Hold** Shift on your keyboard and select every instance except for the dummy transistors.
- After selecting the 3 transistors and resistor like the figure below, head over to the **Parasitics & Electrical Setup** assistant on the right and click on **Select Inst-Terms** from the drop-down arrow and click on the icon near the drop-down arrow.



- Note that Select Inst-Terms will select all the device's terminals.
- Make sure that the schematics view is in Editing mode.

2.b) Signal Selection To Save Current (Continued)

- The Schematics XL and **Parasitics & Electrical Setup** assistant should now look like this.
- As seen in the image below, a new selection setup with the default name “ElectricalSetup_SignalSelection” is produced and added to the design's list.

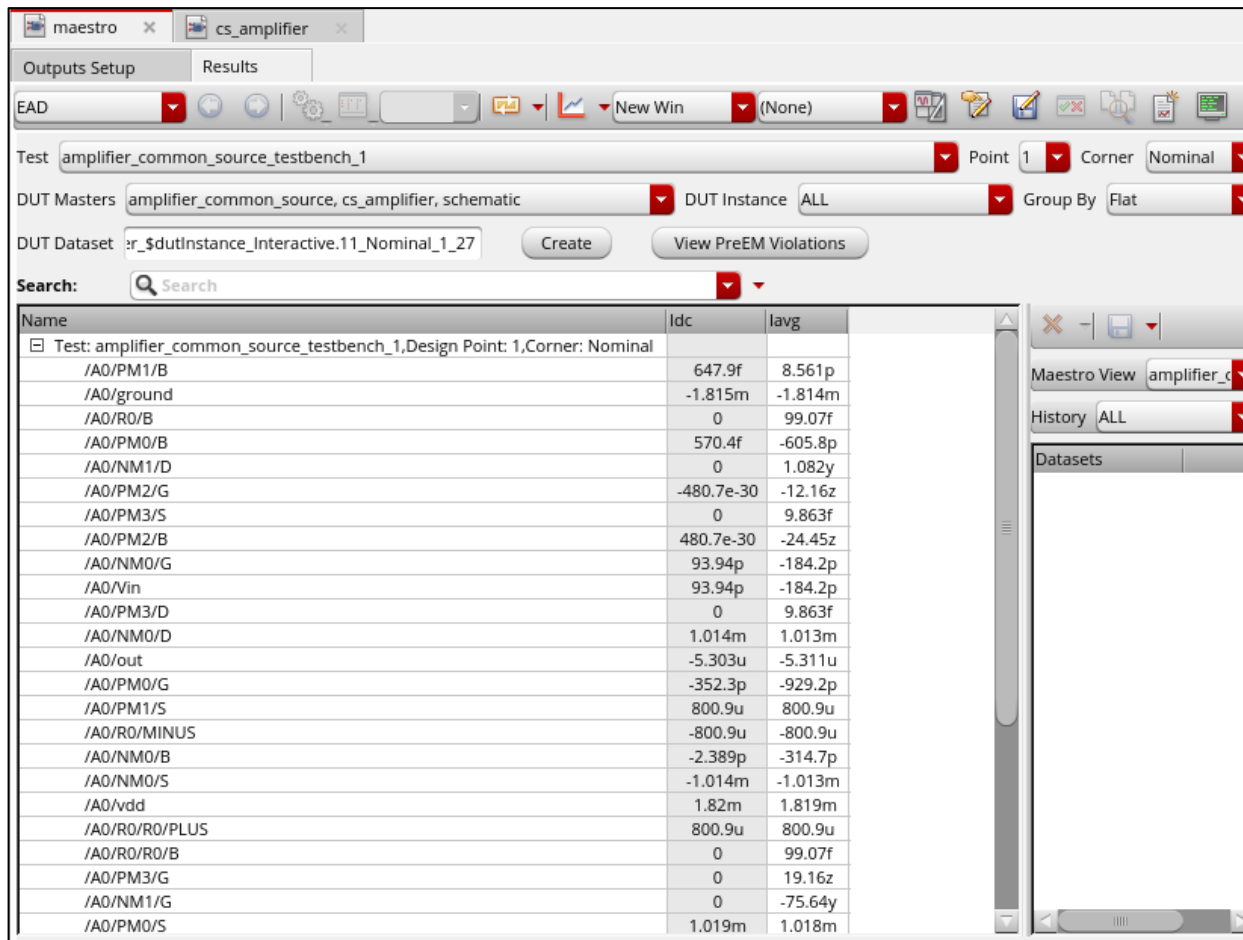


- Note that It's okay if the yellow lines that show up after choosing the components don't look exactly like the figure.

2.c) Creating Datasets

- Open the maestro view again and **Run** the simulation.
- After the simulation is finished, the EAD is displayed.

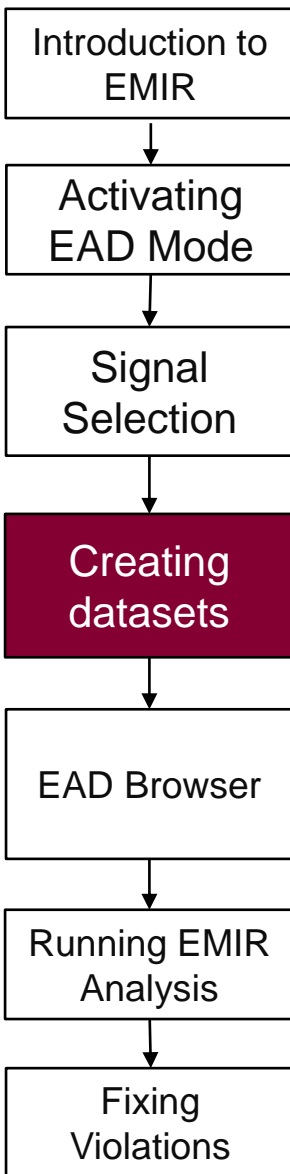
- Make sure ALL the runs are completed.



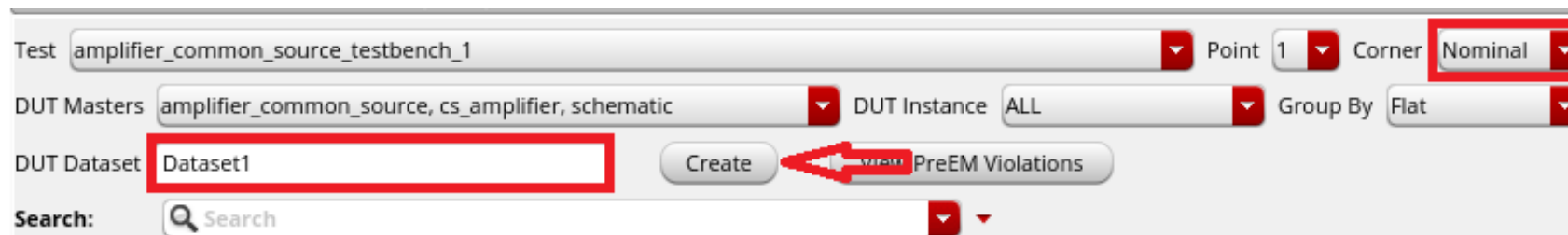
The screenshot shows the Cadence Maestro EAD Browser interface. The main window displays a table of simulation results for the testbench 'amplifier_common_source_testbench_1' at Design Point 1, Corner: Nominal. The table lists various signals and their values for Idc and Iavg. The 'DUT Dataset' is set to 'r_\$dutInstance_Interactive.11_Nominal_1_27'.

Name	Idc	Iavg
Test: amplifier_common_source_testbench_1, Design Point: 1, Corner: Nominal		
/A0/PM1/B	647.9f	8.561p
/A0/ground	-1.815m	-1.814m
/A0/R0/B	0	99.07f
/A0/PM0/B	570.4f	-605.8p
/A0/NM1/D	0	1.082y
/A0/PM2/G	-480.7e-30	-12.16z
/A0/PM3/S	0	9.863f
/A0/PM2/B	480.7e-30	-24.45z
/A0/NM0/G	93.94p	-184.2p
/A0/Vin	93.94p	-184.2p
/A0/PM3/D	0	9.863f
/A0/NM0/D	1.014m	1.013m
/A0/out	-5.303u	-5.311u
/A0/PM0/G	-352.3p	-929.2p
/A0/PM1/S	800.9u	800.9u
/A0/R0/MINUS	-800.9u	-800.9u
/A0/NM0/B	-2.389p	-314.7p
/A0/NM0/S	-1.014m	-1.013m
/A0/vdd	1.82m	1.819m
/A0/R0/R0/PLUS	800.9u	800.9u
/A0/R0/R0/B	0	99.07f
/A0/PM3/G	0	19.16z
/A0/NM1/G	0	-75.64y
/A0/PM0/S	1.019m	1.018m

2.c) Creating Datasets (continued)

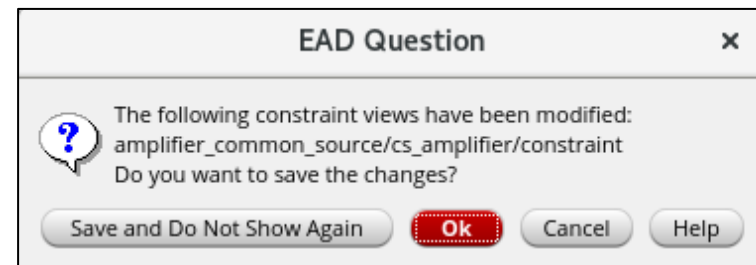
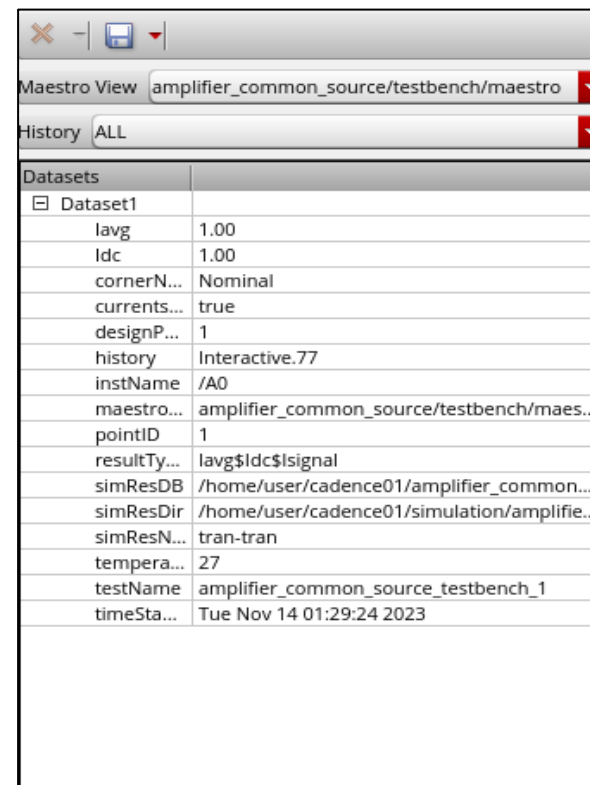


- For our EMIR analysis, we need to use the current data in the layout.
- For that reason, we save the selected current data in Datasets, which will be then used in .
- First, we should name our Dataset. In the **DUT Dataset** field, replace the default name “*cs_amplifier_\$dutInstance_Interactive._Nominal_1_27*” with “*Dataset1*”.
- We will leave the corner as **nominal**.
- Finally, to create the Dataset, click on the **create** button.



2.c) Creating Datasets (continued)

- If the following question pops up, click on **OK**.
- The Dataset we just created will be shown on the right under Datasets.

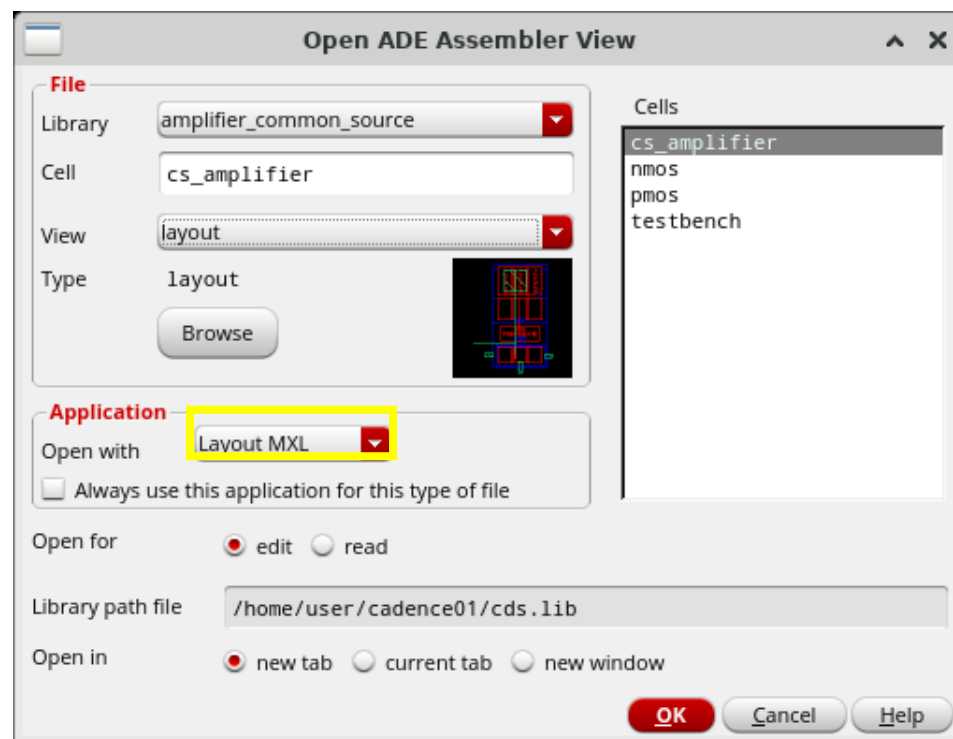



Datasets	
Dataset1	
lavg	1.00
ldc	1.00
cornerN...	Nominal
currents...	true
designP...	1
history	Interactive.77
instName	/A0
maestro...	amplifier_common_source/testbench/maes...
pointID	1
resultTy...	lavg\$ldc\$signal
simResDB	/home/user/cadence01/amplifier_common...
simResDir	/home/user/cadence01/simulation/amplifie...
simResN...	tran-tran
tempera...	27
testName	amplifier_common_source_testbench_1
timeSta...	Tue Nov 14 01:29:24 2023

3. Performing Electromigration Analysis

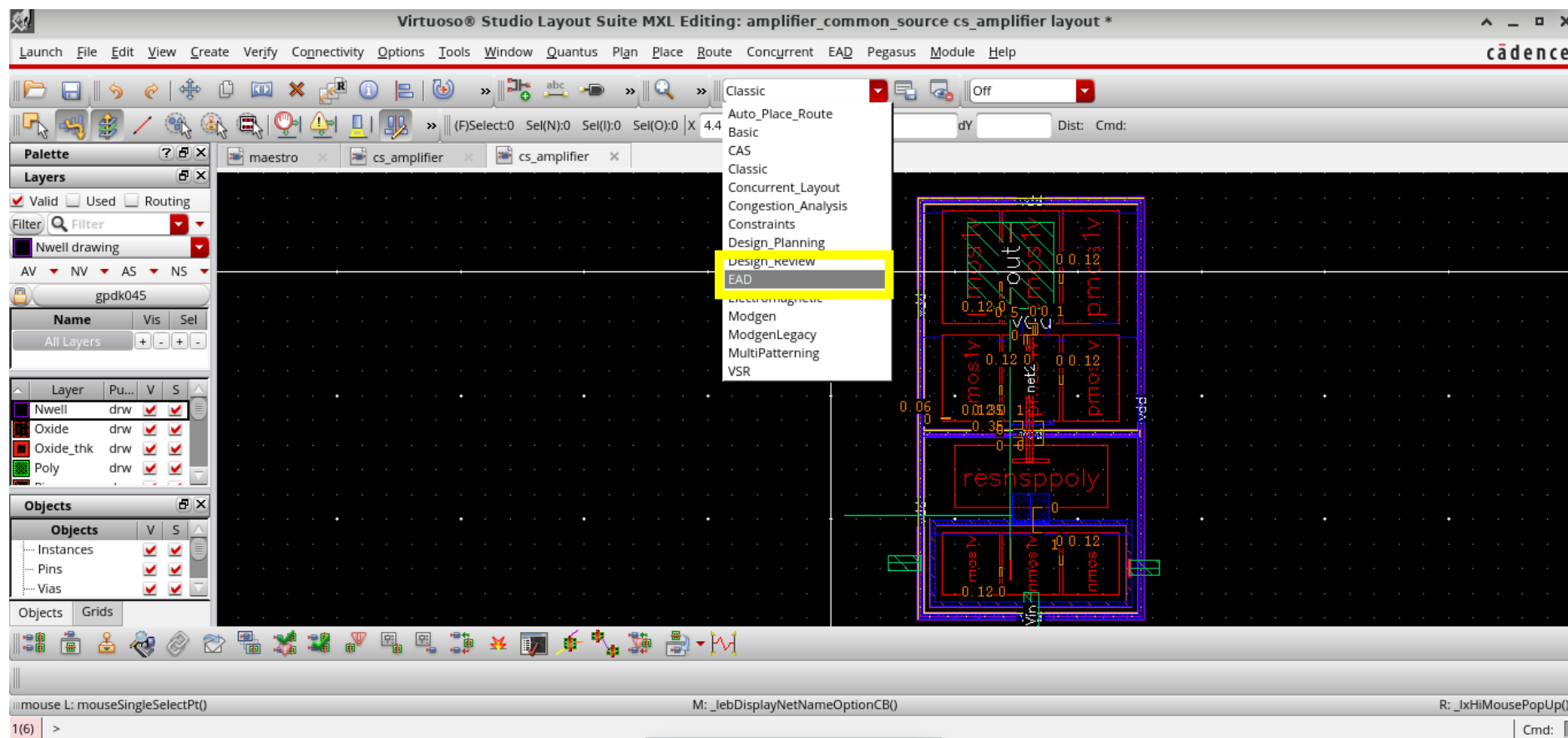
3.a) Setting Up EAD Browser –

- From the upper tabs, click on **File -> Open...**
- Select the **amplifier_common_source** library, and the **cs_amplifier** cell.
- Next to view, select **Layout**.
- Under Application, make sure to open with **Layout MXL**.



3.a) Setting Up EAD Browser –

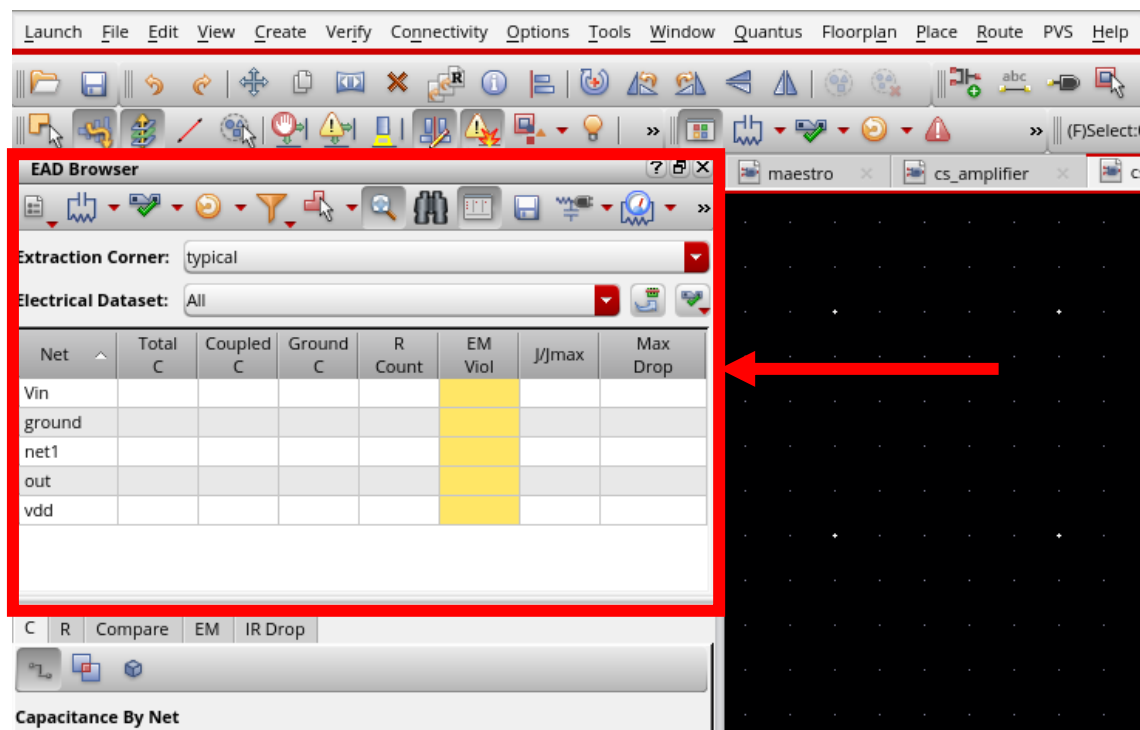
- Then from the upper tabs, click on **Launch -> Layout MXL**
- Change the **Workspace Configuration** to **EAD**.



- If the EAD configuration fails to launch, double check that the EAD pdk configuration files are correctly set.

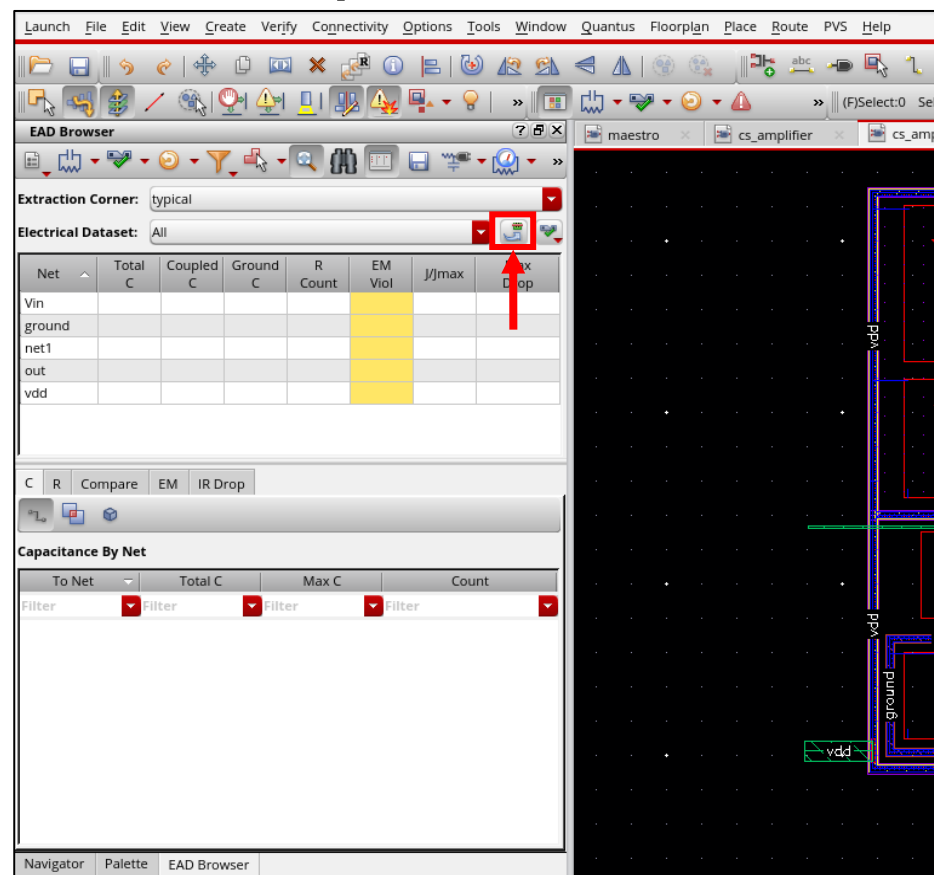
3.a) Setting Up EAD Browser –

- We get the following **EAD Browser** window.



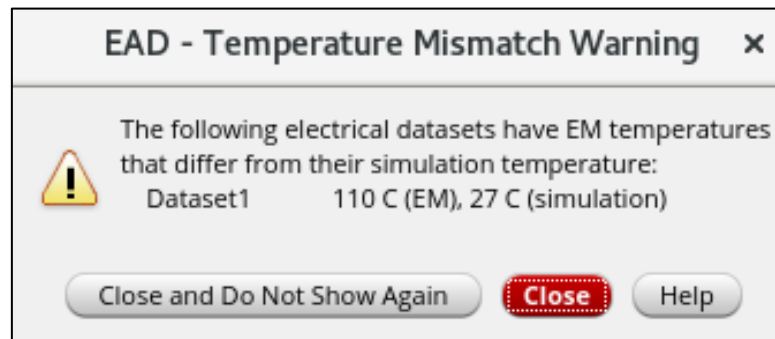
3.a) Setting Up EAD Browser –

- The EAD Browser will now open on the left side like in the figure below.
- For datasets that have changed in ADE Assembler since the datasets were last transferred to the layout, click on the **Update with latest electrical data** button to reload the electrical data.

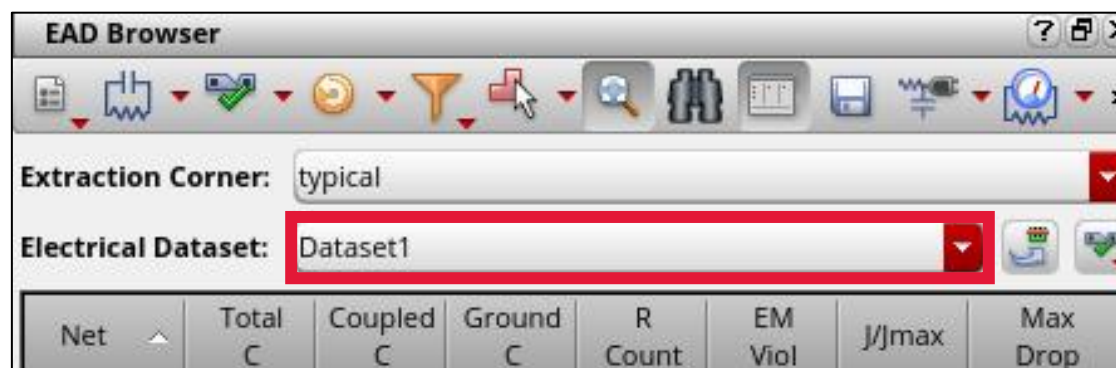


3.a) Setting Up EAD Browser –

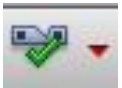
- If this Message shows up, click on **Close**.



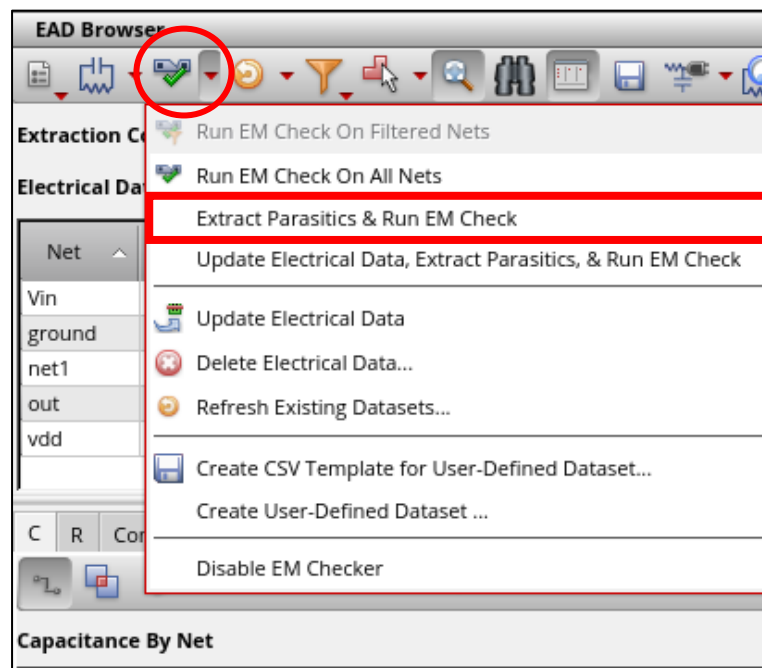
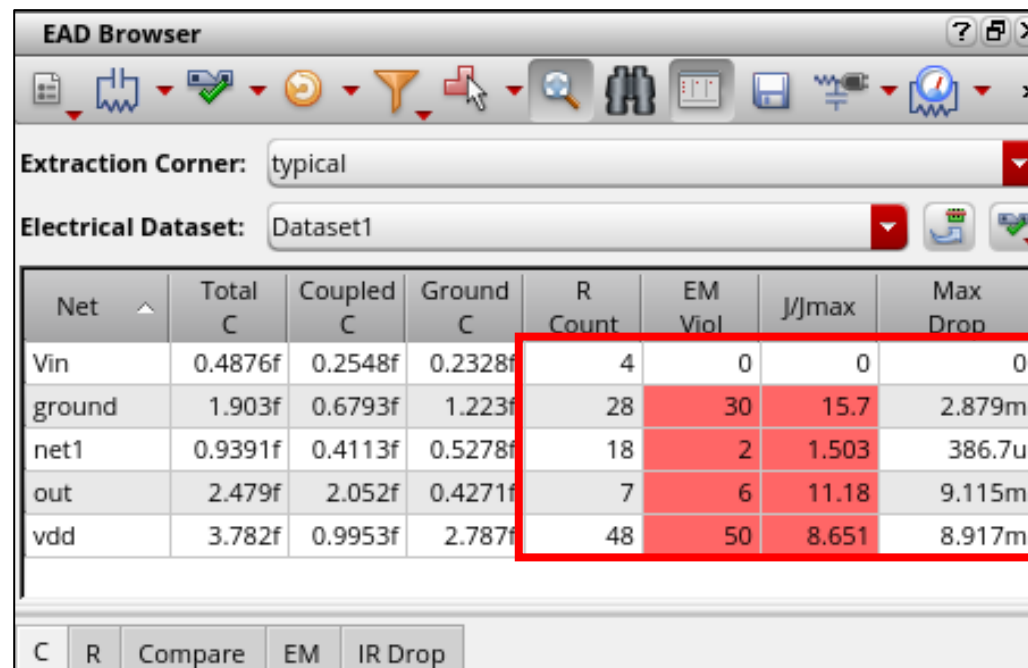
- In the Electrical Dataset field, select the Dataset that we created earlier **Dataset1**.



3.b) Extracting Parasitics and Running EM Check

- To run the EM analysis, we will first extract the parasitics and then run the EM check.
- We can do that by clicking on the drop-down arrow of the **EM checker** button and selecting **Extract Parasitics & Run EM Check**. 
- The image on the right shows the results.

- Keep in mind that it's acceptable to proceed if your values are slightly different.

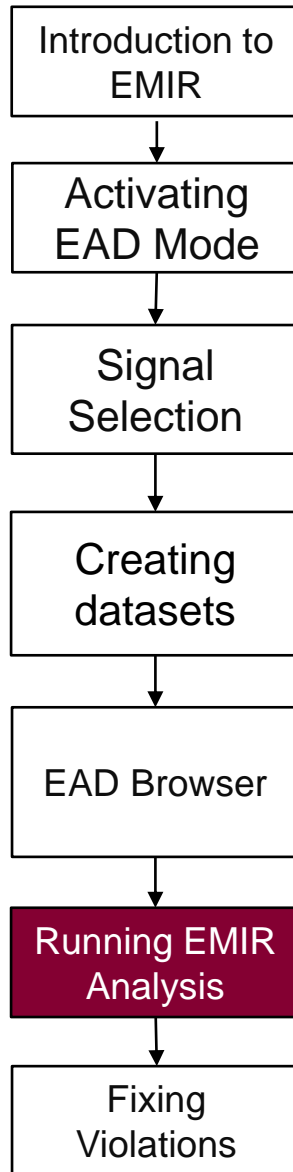



The screenshot shows the EAD Browser window with the 'Electrical Dataset' set to 'Dataset1'. The results table is displayed, showing various metrics for different nets. The table has columns: Net, Total C, Coupled C, Ground C, R Count, EM Viol, J/Jmax, and Max Drop. The 'ground' and 'vdd' rows are highlighted in red.

Net	Total C	Coupled C	Ground C	R Count	EM Viol	J/Jmax	Max Drop
Vin	0.4876f	0.2548f	0.2328f	4	0	0	0
ground	1.903f	0.6793f	1.223f	28	30	15.7	2.879m
net1	0.9391f	0.4113f	0.5278f	18	2	1.503	386.7u
out	2.479f	2.052f	0.4271f	7	6	11.18	9.115m
vdd	3.782f	0.9953f	2.787f	48	50	8.651	8.917m

3.b) Extracting Parasitics and Running EM Check

- EAD updates the summary table with color-coded electromigration data for the design's nets after the check is complete.
- Red shows that there are violations concerning Electromigration.
- For every net, **EM Viol** displays the total amount of electromigration violations.
- **J/Jmax** displays the worst-case current to maximum current ratio. There is a violation if the value is larger than or equal to 1.0.
- **Max Drop** displays the maximum IR drop across a net between two terminals.



4. Fixing Violations

4. Fixing Violations

- After completing the EMIR analysis, it is time to optimize the design to get rid of the EM violations.
- To achieve that, we will expand the impacted metals' areas until their **J/Jmax** values are **lower than 1**.
- For this module, we are going to fix the violations for the **net1** and **out** nets.
- Click on one of the **net1**'s cells (EM Viol or J/Jmax) in the summary pane to open the EM tab in the details pane.

EAD Browser

Extraction Corner: typical

Electrical Dataset: Dataset1

Net	Total C	Coupled C	Ground C	R Count	EM Viol	J/Jmax	Max Drop
Vin	0.4876f	0.2548f	0.2328f	4	0	0	0
ground	1.903f	0.6793f	1.223f	28	30	15.7	2.879m
net1	0.9391f	0.4113f	0.5278f	18	2	1.503	386.7u
out	2.479f	2.052f	0.4271f	7	6	11.18	9.115m
vdd	3.782f	0.9953f	2.787f	48	50	8.651	8.917m

C R Compare EM IR Drop

Worst-case

EM Results (net1, 2 violations)

R	J/Jmax Worstcase	J/Jmax Static-Avg	J/Jmax DC Op Current	Layer	W	L
388.5m	1.503	1.503	1.503	Metal2	0.3	1.55
45.45m	606.7m	606.7m	606.7m	Via1		
45.45m	606.7m	606.7m	606.7m	Via1		

Navigator Palette EAD Browser

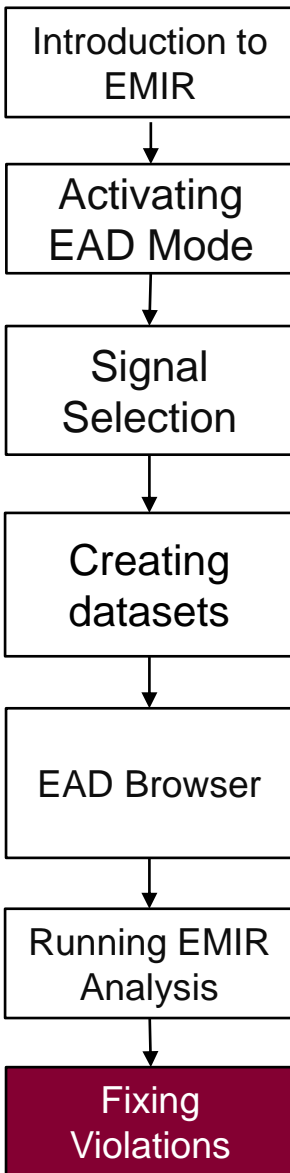
- Note that the **net** number may differ.

4. Fixing Violations

- In the detail pane, we can see the resistance values in the **R** column.
- The results displayed show the values of J/Jmax for the Current from the DC Operating Point analysis (**DC Op Current**) and for Average current from the transient analysis (**Static-Avg**).
- The number of EM violations ($J/J_{max} > 1$) for net1 is 2 and they are shown in the details pane below.

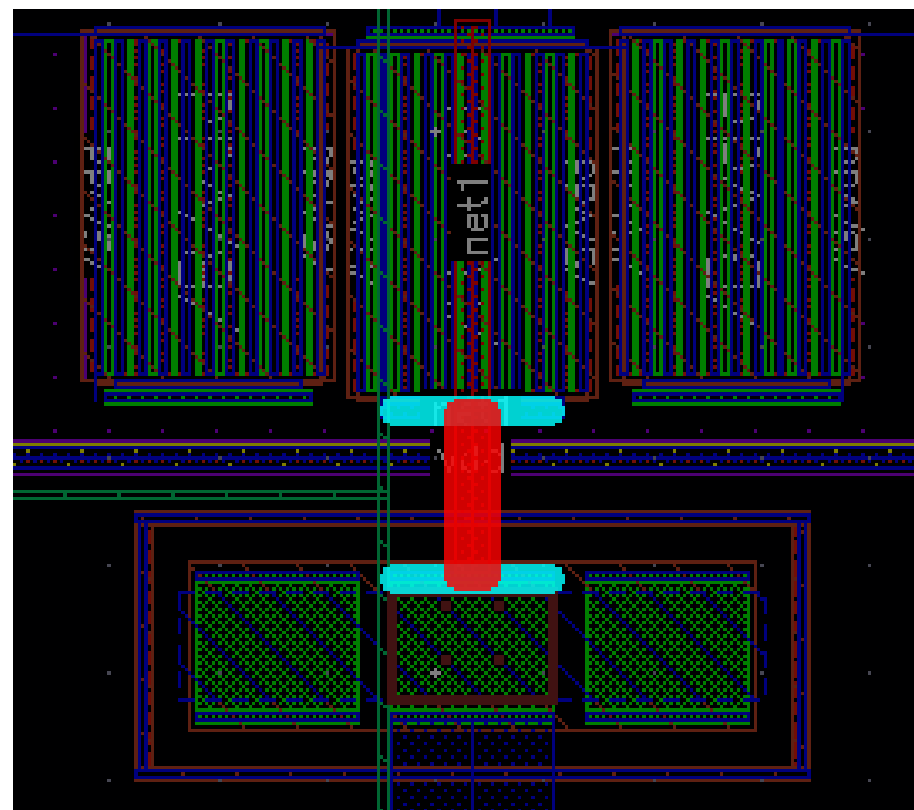
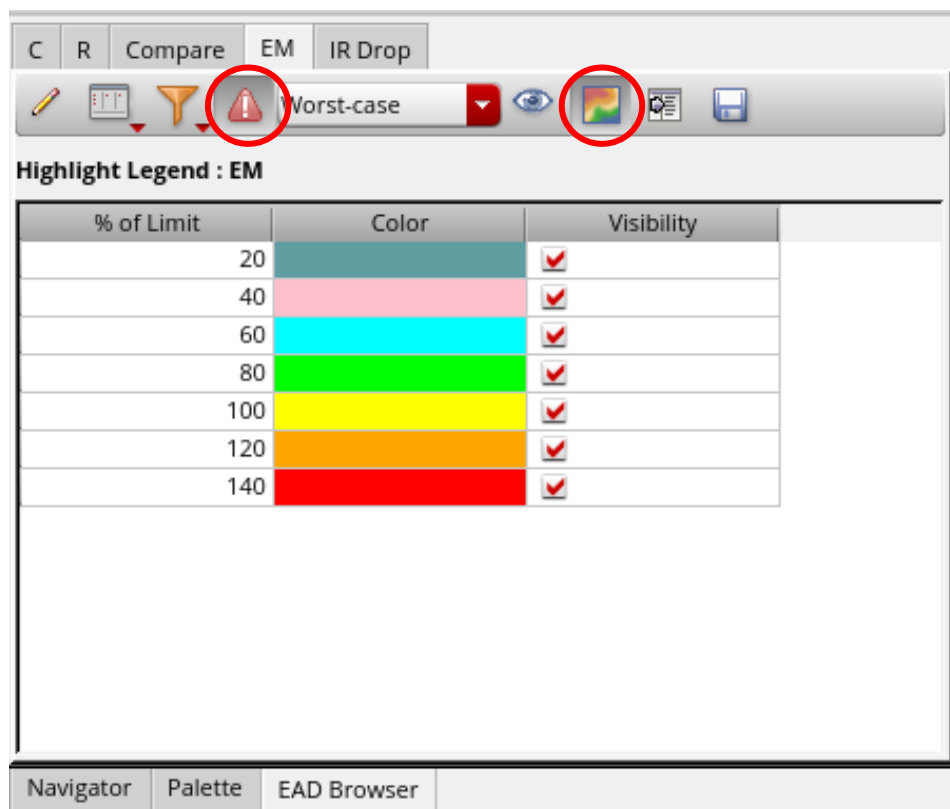
EM Results (net1, 2 violations)

R	J/Jmax Worstcase	J/Jmax Static-Avg	J/Jmax DC Op Current	Layer	W	L
388.5m	1.503	1.503	1.503	Metal2	0.3	1.55
45.45m	606.7m	606.7m	606.7m	Via1		
45.45m	606.7m	606.7m	606.7m	Via1		



4. Fixing Violations

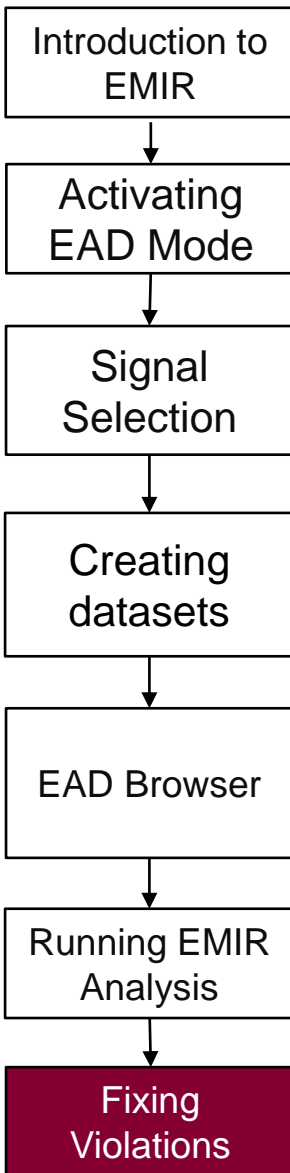
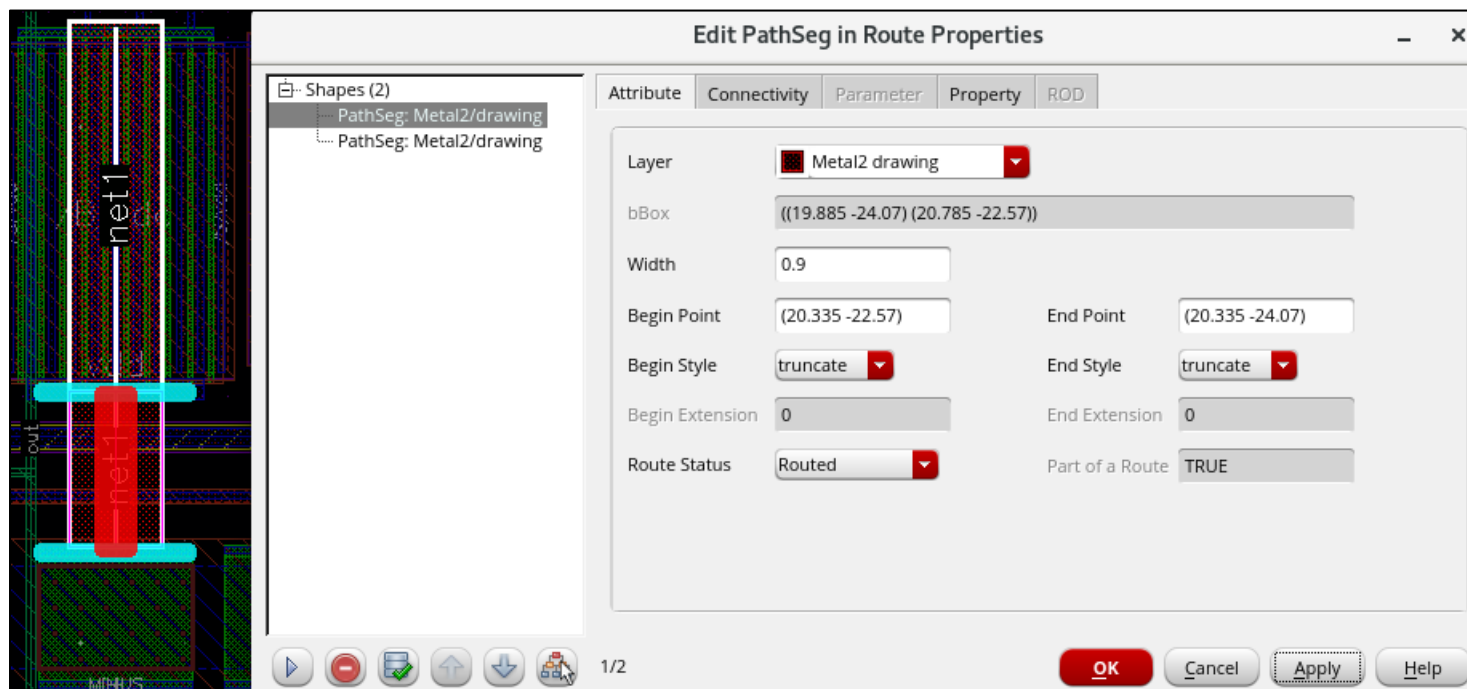
- To identify EM hot spots (violations) click on Highlight EM Violations.
- Click **Show Legend Table** which shows the ranges of EM violations that are used in the EAD to indicate violations.




- Note that clicking on Highlight EM Violations will be easier for us to locate the violations and fix them
- Note that anything above 100% in the Table is considered a violation and should be fixed

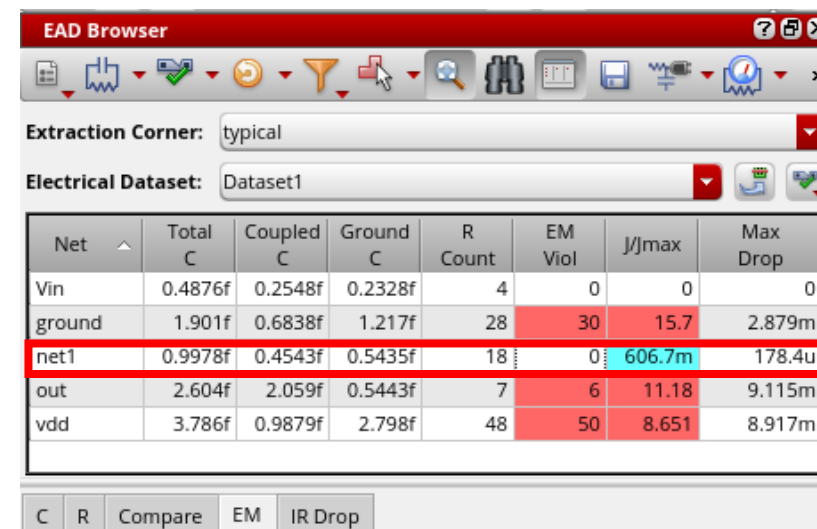
4. Fixing Violations

- Select the net1 and press Q to open the net's properties.
- Change the width from 0.3 to 0.9 and press OK.



4. Fixing Violations

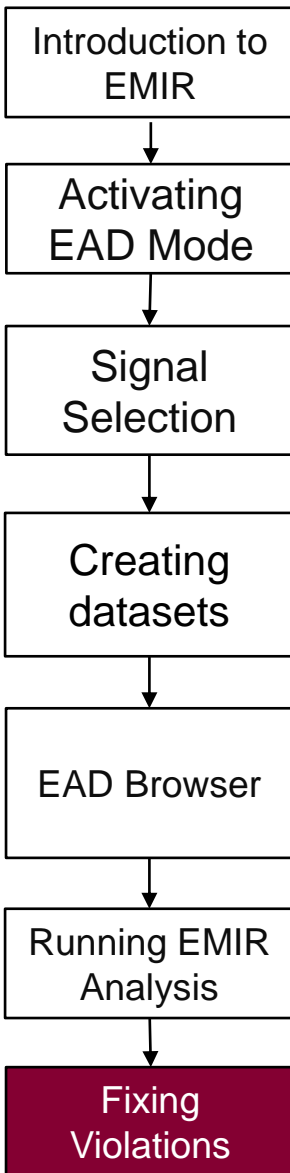
- Click **Update Parasitics & EM** in the summary tab to update the results. 
- As we can see, there is no EM Violations anymore and the IR Drop was reduced from 386.7u to 178.4u.

The screenshot shows the EAD Browser window with the results table. The 'net1' row is highlighted in red, indicating it has no EM violations and a reduced IR drop.

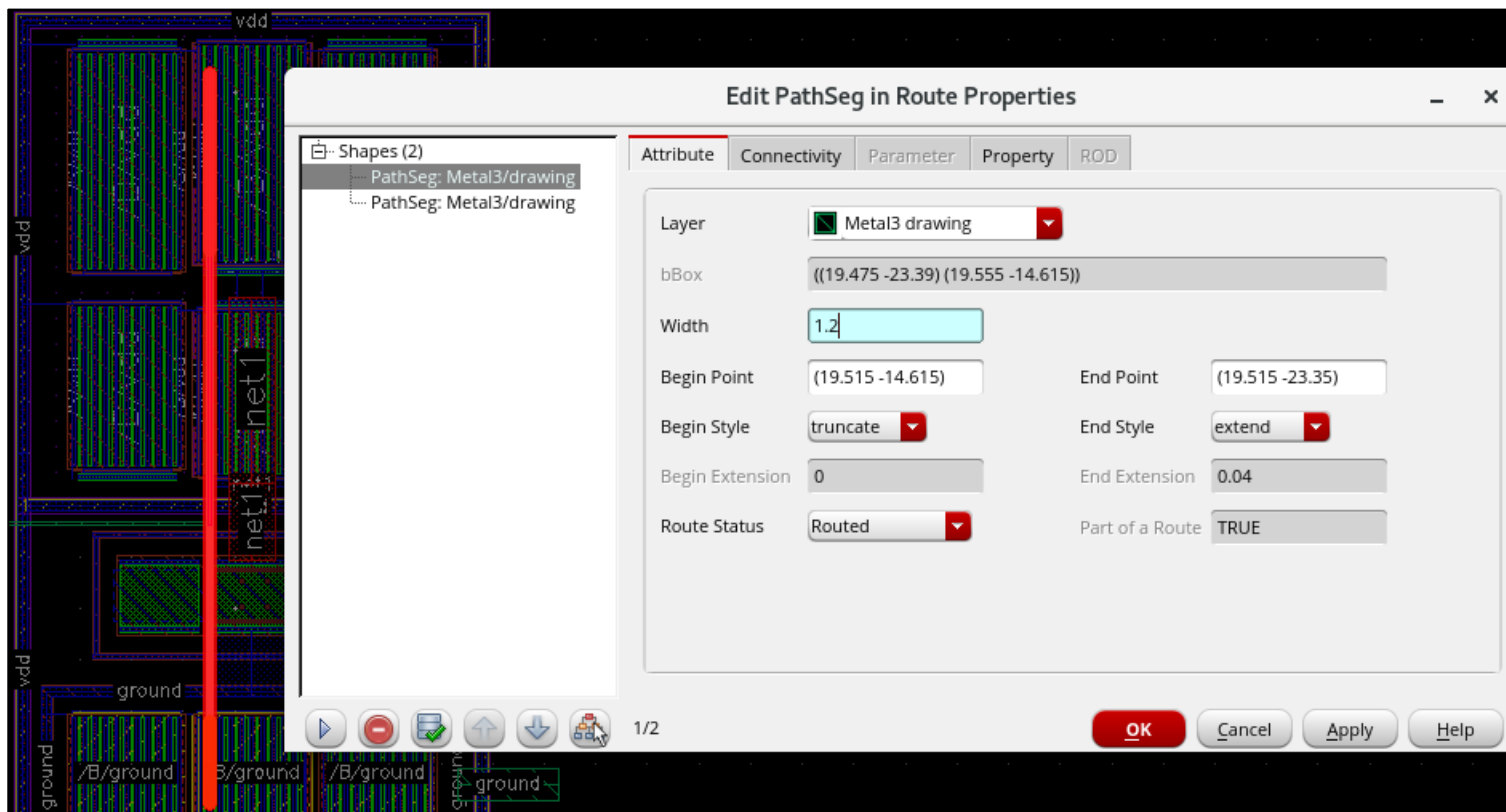
Net	Total C	Coupled C	Ground C	R Count	EM Viol	I/Jmax	Max Drop
Vin	0.4876f	0.2548f	0.2328f	4	0	0	0
ground	1.901f	0.6838f	1.217f	28	30	15.7	2.879m
net1	0.9978f	0.4543f	0.5435f	18	0	606.7m	178.4u
out	2.604f	2.059f	0.5443f	7	6	11.18	9.115m
vdd	3.786f	0.9879f	2.798f	48	50	8.651	8.917m

At the bottom of the window, the 'IR Drop' tab is selected.



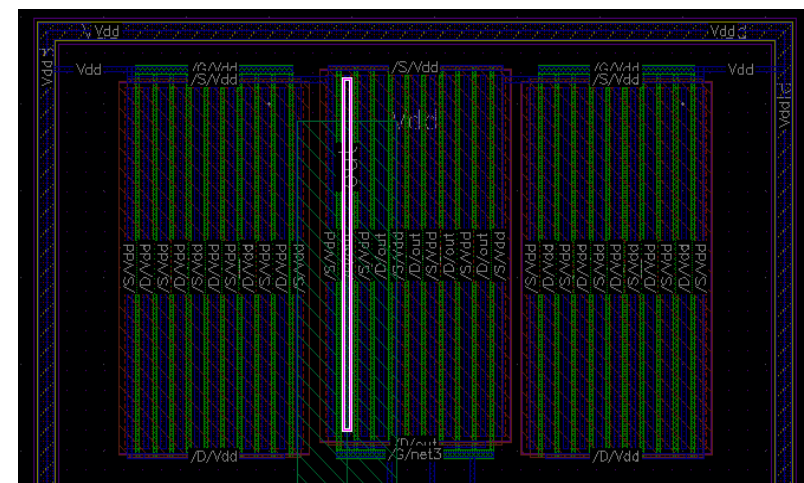
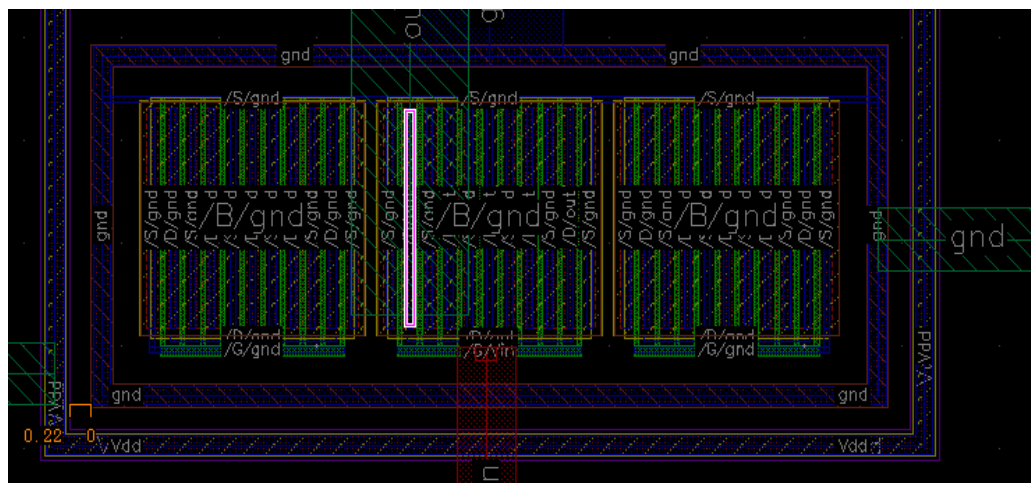
4. Fixing Violations

- Select the vertical Output path and press Q.
- Change the width from 0.08 to 1.02 and click OK.



4. Fixing Violations

- Select the lower Via stack of Metal1 to Metal 3 and change the rows from 12 to 15.
- Select the upper Via stack of Metal1 to Metal3 and change the rows from 25 to 29.
- Make sure to adjust their position as shown below.



- Note that you must pick the Via and click Q to adjust its settings if you would like to change how many rows it has.

Introduction to
EMIR

Activating
EAD Mode

Signal
Selection

Creating
datasets

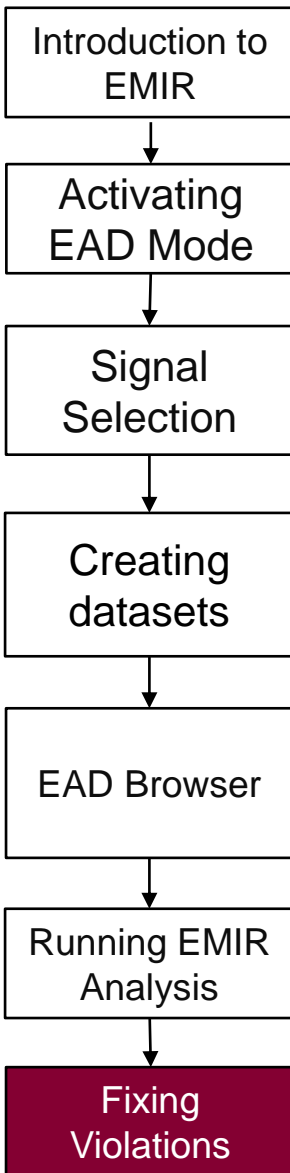
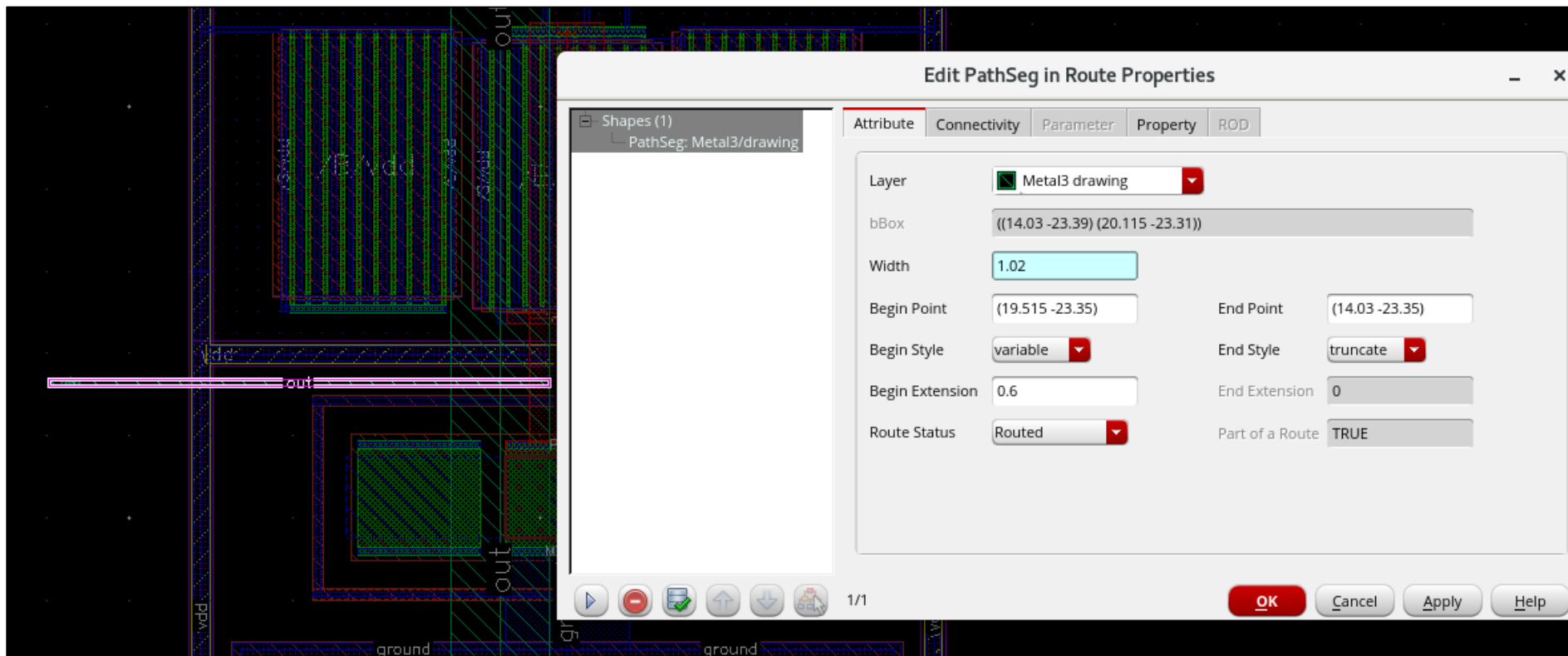
EAD Browser

Running EMIR
Analysis

Fixing
Violations

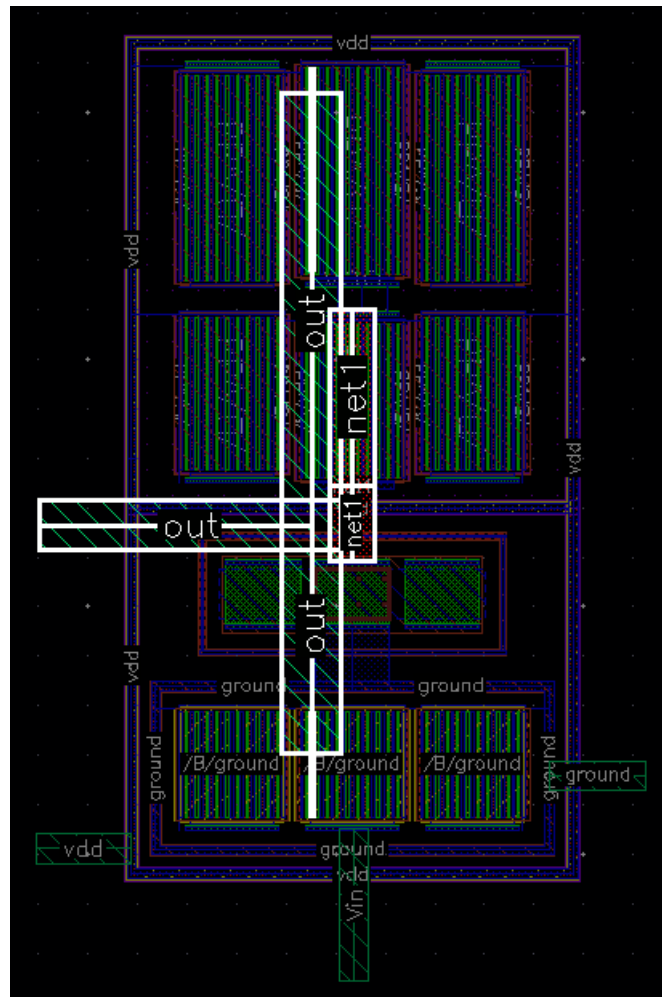
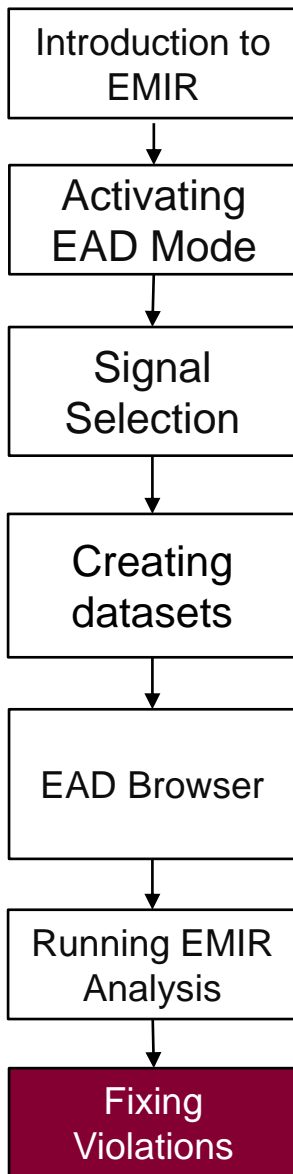
4. Fixing Violations

- Select the horizontal Output path and change its width from 0.08 to 1.02.




4. Fixing Violations

- The layout should look like this.



4. Fixing Violations

- Save the layout and rerun the EM check by pressing **Update parasitics & EM.** 
- As we can see, the IR Drop for the **out** net was reduced from 9.115m to 850.8u, and there are no longer any EM Violations for net1 and out.

EAD Browser

Extraction Corner: typical

Electrical Dataset: Dataset1

Net	Total C	Coupled C	Ground C	R Count	EM Viol	I/Jmax	Max Drop
Vin	0.5267f	0.2946f	0.232f	4	0	0	0
ground	2.12f	0.8332f	1.287f	28	30	15.7	2.879m
net1	1.273f	0.5596f	0.7138f	18	0	606.7m	178.4u
out	4.701f	3.828f	0.873f	11	0	845m	850.8u
vdd	5.148f	2.352f	2.796f	48	50	8.651	8.917m

C R Compare EM IR Drop