

# Virtuoso 23.1

## Module 12 – Post-Layout Simulations

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Lebanon

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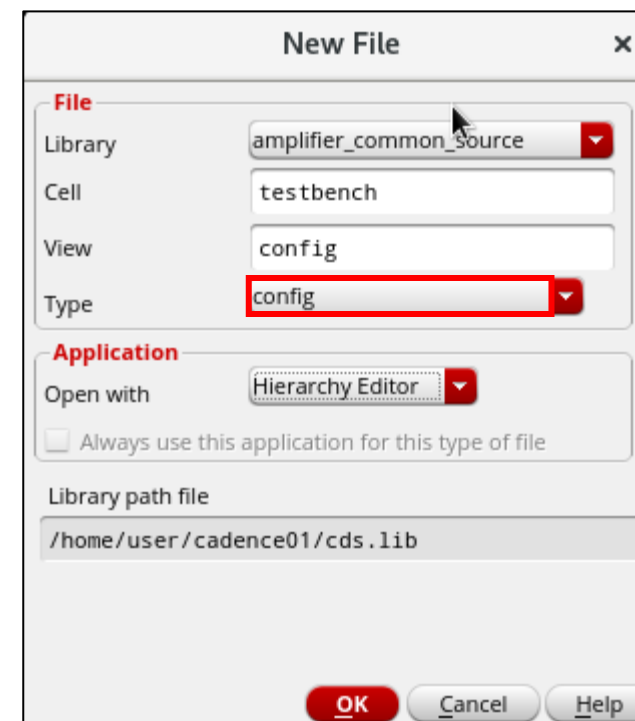
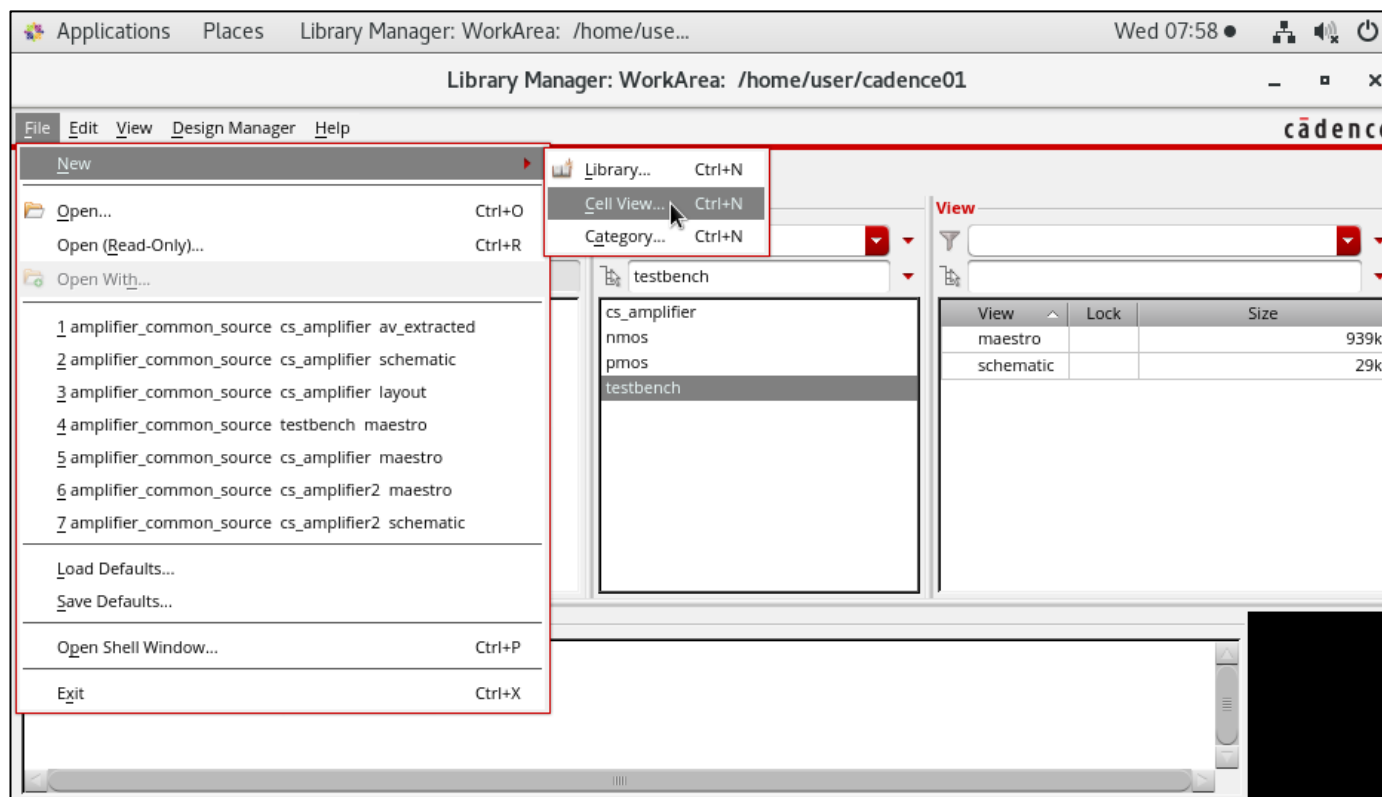
# Module Objective

In this module, we will learn how to use the extracted view to simulate the circuit with the parasitics.

# 1. Setting up the Configuration View

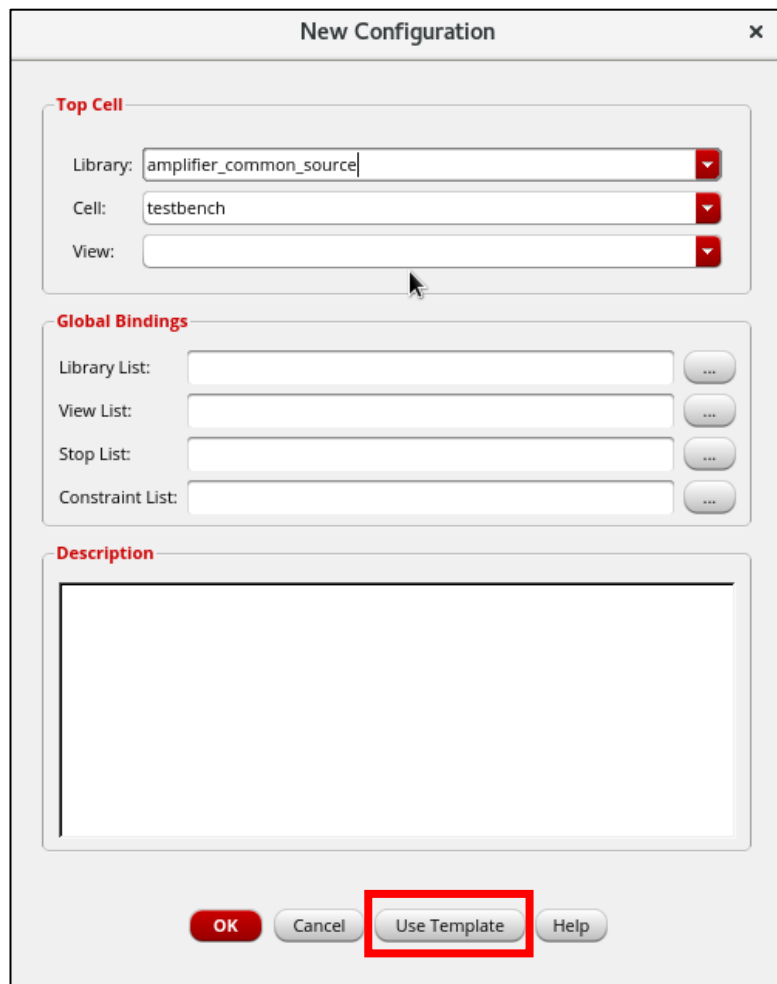
# 1. Setting up the Configuration View

- First, we must set a new configuration to our symbol view. From the **Library Manager**, click on the library **amplifier\_common\_source**, then click on the **testbench** cell, then **File → New → Cell View...**
- Change the Type to “**config**”, and make sure the Library and the Cell fields are as shown below.



# 1. Setting up the Configuration View *(continued)*

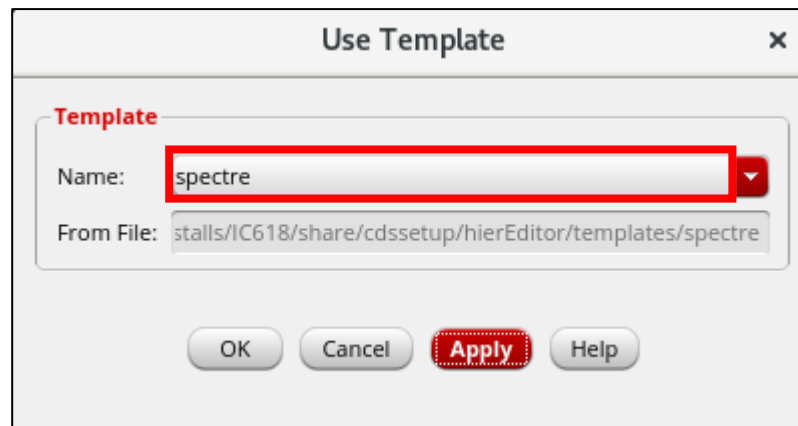
- The New Configuration window opens.
- Click on **Use Template**. From the drop-down list of the “Name” field choose **spectre**.



The "New Configuration" dialog box is shown. It has a title bar with a close button. The main area is divided into three sections: "Top Cell", "Global Bindings", and "Description".

- Top Cell:** Contains three dropdown menus: "Library:" (set to "amplifier\_common\_source"), "Cell:" (set to "testbench"), and "View:" (empty).
- Global Bindings:** Contains four text input fields with "..." buttons: "Library List:", "View List:", "Stop List:", and "Constraint List:".
- Description:** A large empty text area.

At the bottom, there are four buttons: "OK", "Cancel", "Use Template" (highlighted with a red box), and "Help".



The "Use Template" dialog box is shown. It has a title bar with a close button. The main area is divided into two sections: "Template" and "From File".

- Template:** Contains a "Name:" dropdown menu (set to "spectre" and highlighted with a red box) and a "From File:" text input field (set to "stalls/IC618/share/cdssetup/hierEditor/templates/spectre").

At the bottom, there are four buttons: "OK", "Cancel", "Apply" (highlighted with a red box), and "Help".

# 1. Setting up the Configuration View (*continued*)

- Change the View to **schematic** and click OK.



**New Configuration**

**Top Cell**

Library: amplifier\_common\_source

Cell: testbench

View: schematic

**Global Bindings**

Library List: myLib

View List: ios\_sch cmos.sch schematic veriloga ahdl pspice dspf

Stop List: spectre

Constraint List:

**Description**

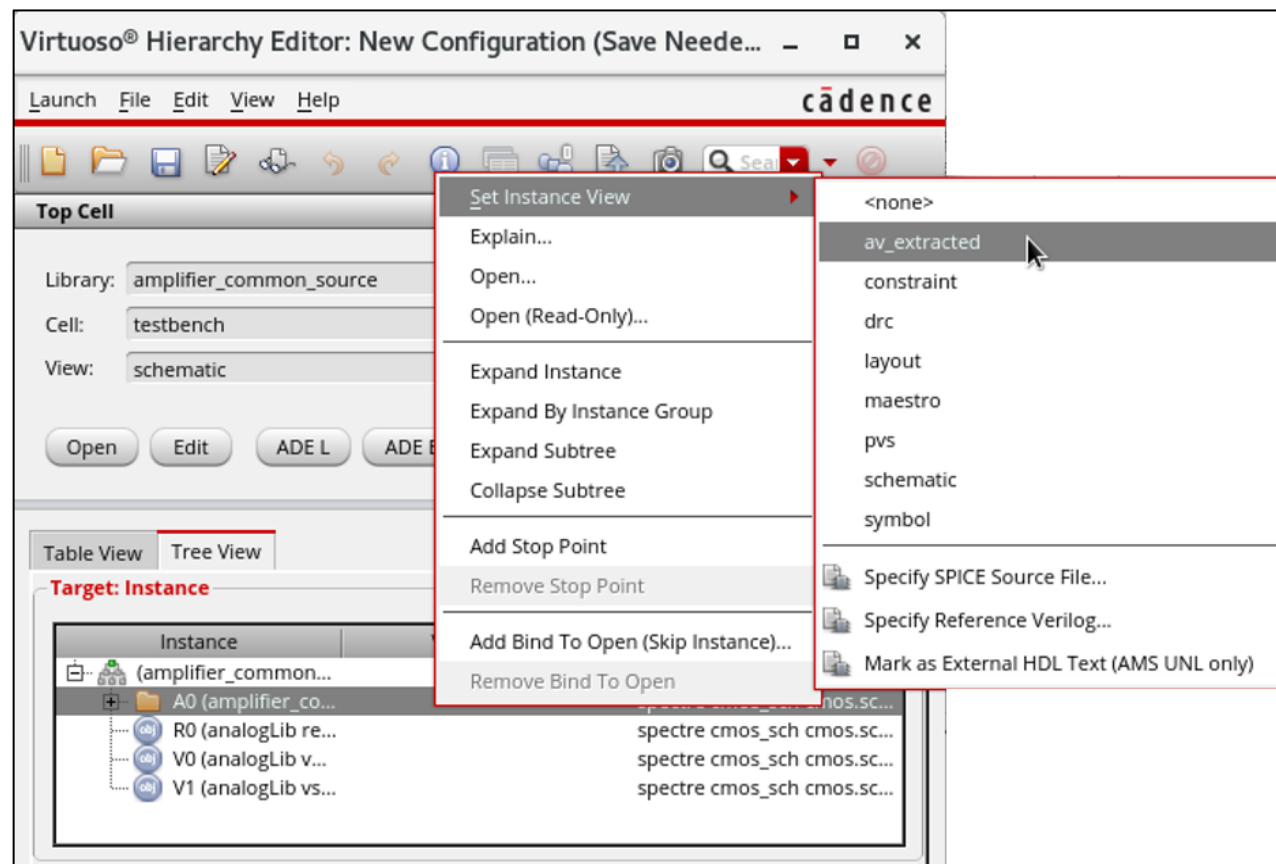
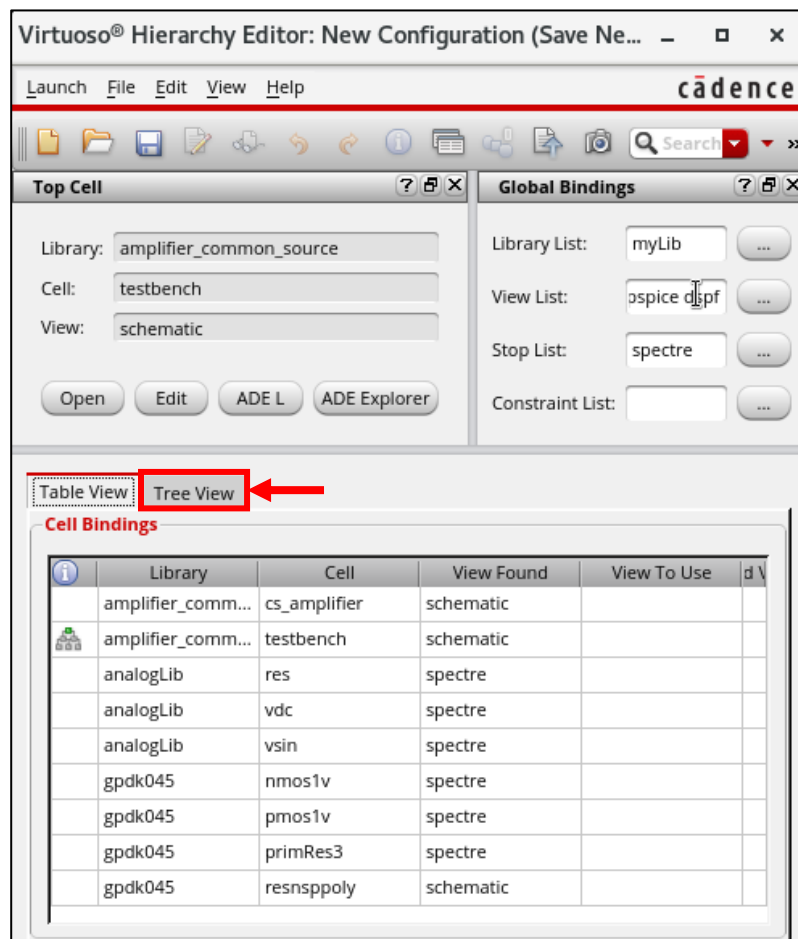
Default template for spectre

Note:  
Please remember to replace Top Cell Library, Cell, and View fields with the actual names used by your design.

OK Cancel Use Template Help

# 1. Setting up the Configuration View (continued)

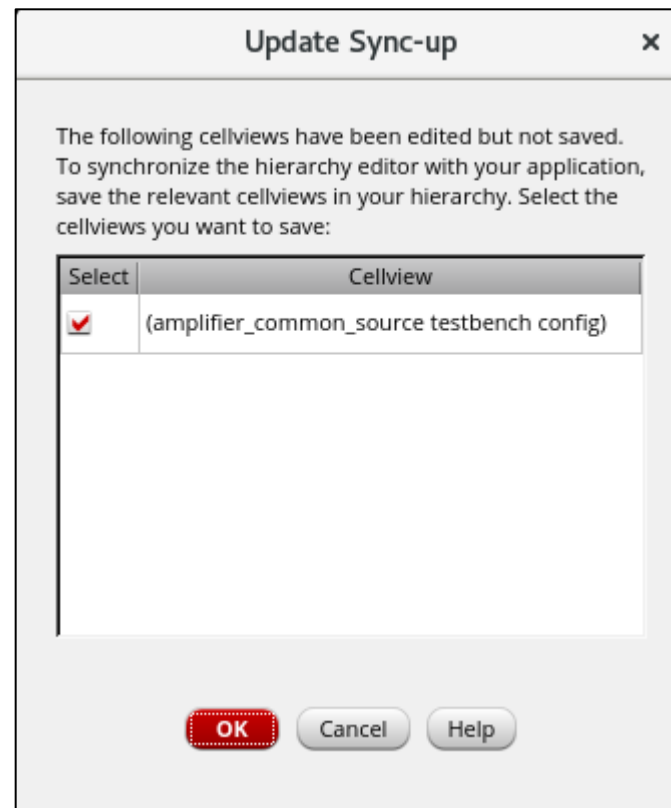
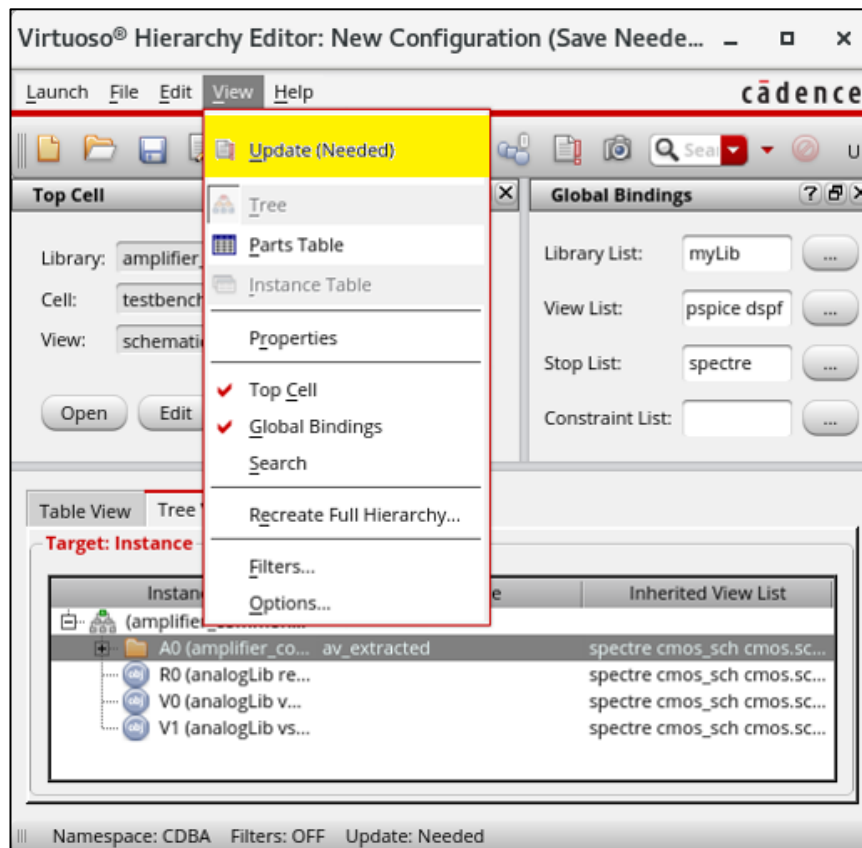
- From the Virtuoso Hierarchy Editor, click on **Tree View**.
- Right click on the folder A0(amplifier\_common\_source cs\_amplifier schematic) → Set Instance View → **av\_extracted**.





# 1. Setting up the Configuration View *(continued)*

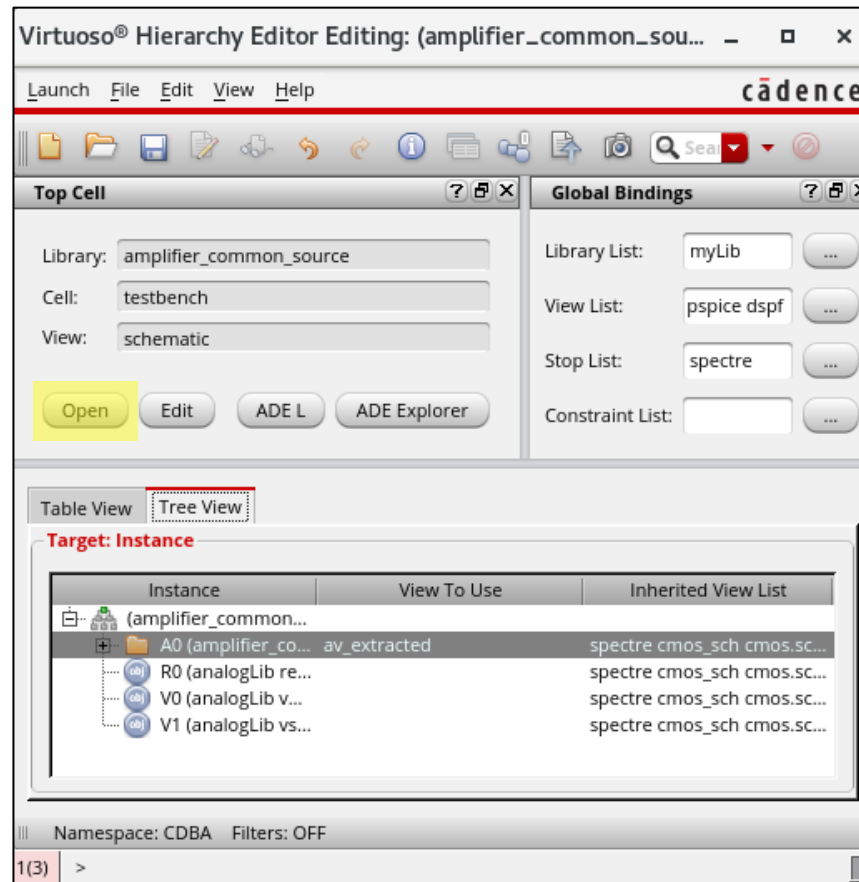
- To update the config file, click on View → Update (Needed).
- The Update Sync-up window pops-up, Click OK, and Save the config file.



## 2. Testbench Modification

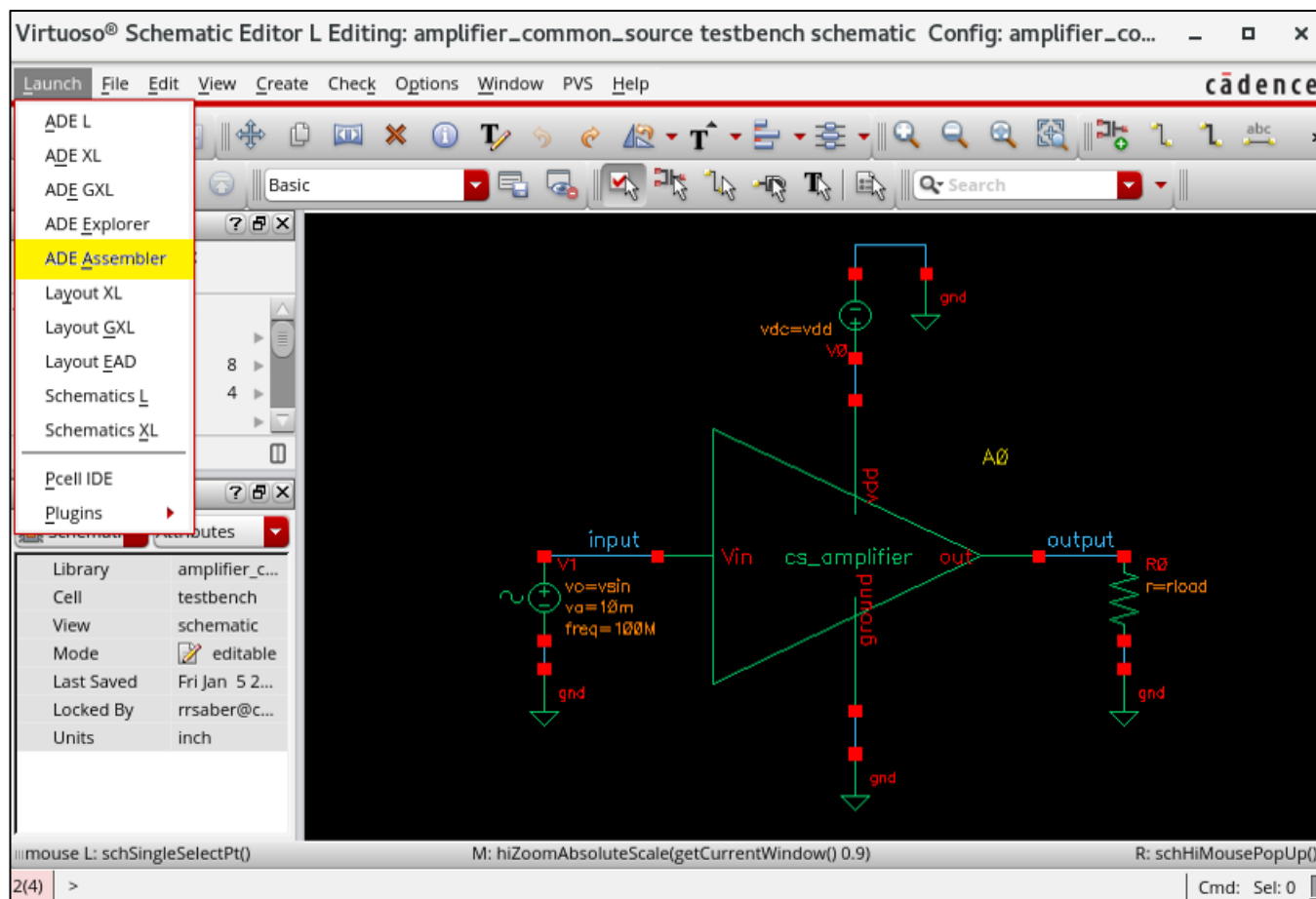
## 2. Testbench Modification

- To open the schematic of the testbench, click on Open (it might take a minute).



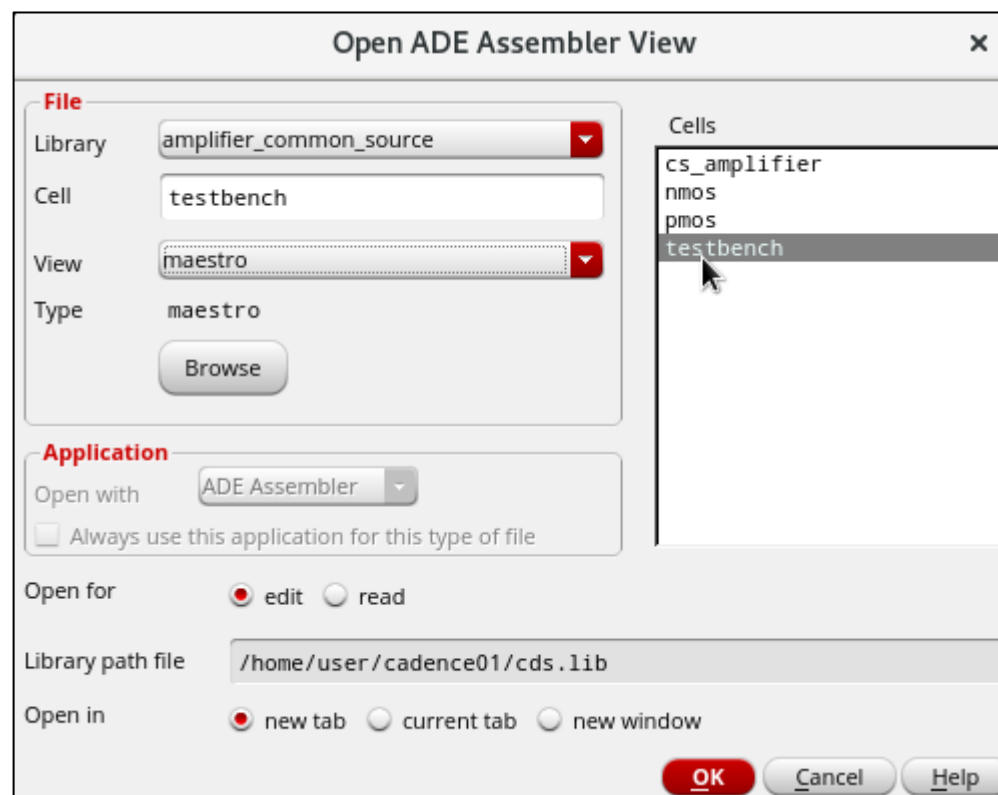
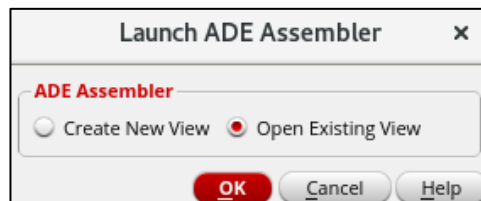
## 2. Testbench Modification (*continued*)

- To simulate the circuit, we will use the tool ADE Assembler. Click Launch → ADE Assembler.



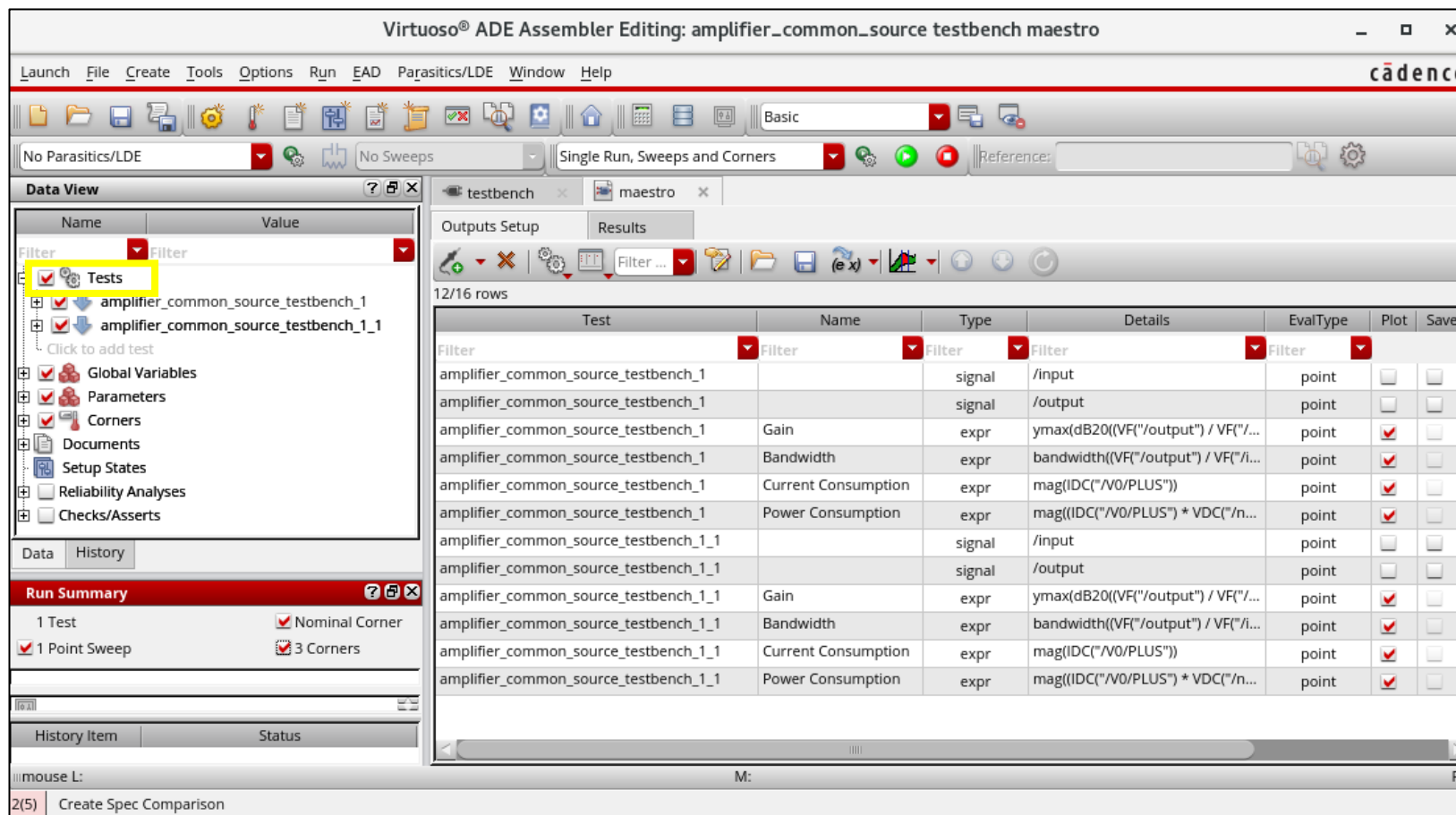
## 2. Testbench Modification (*continued*)

- The Launch ADE Assembler from opens, choose “Open Existing View”, and click OK.
- Make sure the Cell is set to testbench and the View to maestro.
- Click OK to open the tests.



## 2. Testbench Modification (*continued*)

- Notice the tab maestro along with the tab testbench.
- Expand the tab Tests. Notice we already have a copy of the original testbench.
- We will rename the Tests to “testbench\_pre\_layout” and “testbench\_post\_layout”.



Virtuoso® ADE Assembler Editing: amplifier\_common\_source testbench maestro

Launch File Create Tools Options Run EAD Parasitics/LDE Window Help

No Parasitics/LDE No Sweeps Single Run, Sweeps and Corners Reference:

Data View

Name	Value
Filter	Filter
Tests	
amplifier_common_source_testbench_1	
amplifier_common_source_testbench_1_1	

Click to add test

- Global Variables
- Parameters
- Corners
- Documents
- Setup States
- Reliability Analyses
- Checks/Asserts

Run Summary

1 Test ☒ Nominal Corner

1 Point Sweep ☒ 3 Corners

History Item Status

maestro

12/16 rows

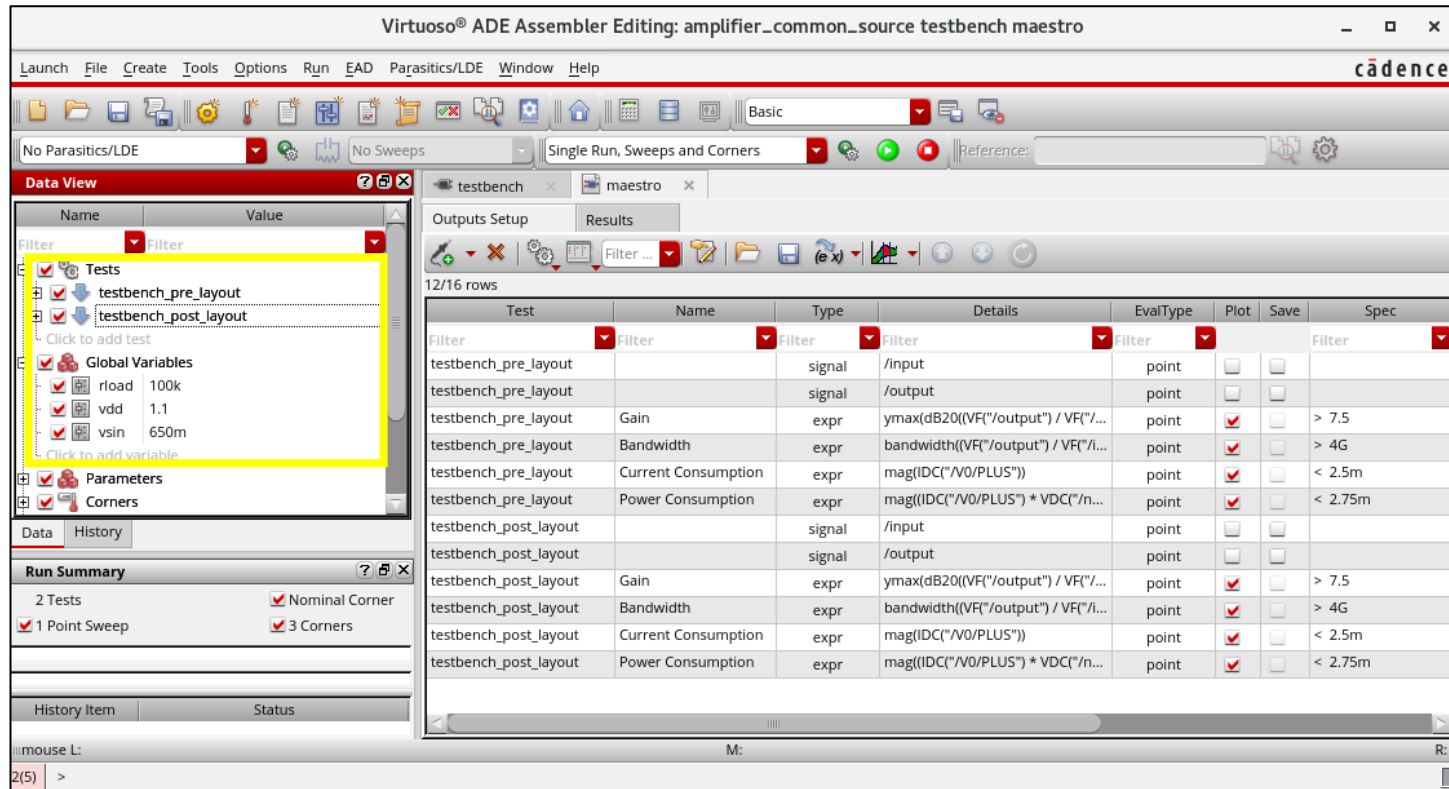
Test	Name	Type	Details	EvalType	Plot	Save
amplifier_common_source_testbench_1		signal	/input	point	<input type="checkbox"/>	<input type="checkbox"/>
amplifier_common_source_testbench_1		signal	/output	point	<input type="checkbox"/>	<input type="checkbox"/>
amplifier_common_source_testbench_1	Gain	expr	ymax(dB20((VF("/output") / VF("/i...))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>
amplifier_common_source_testbench_1	Bandwidth	expr	bandwidth((VF("/output") / VF("/i...))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>
amplifier_common_source_testbench_1	Current Consumption	expr	mag(IDC("/V0/PLUS"))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>
amplifier_common_source_testbench_1	Power Consumption	expr	mag((IDC("/V0/PLUS") * VDC("/n...))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>
amplifier_common_source_testbench_1_1		signal	/input	point	<input type="checkbox"/>	<input type="checkbox"/>
amplifier_common_source_testbench_1_1		signal	/output	point	<input type="checkbox"/>	<input type="checkbox"/>
amplifier_common_source_testbench_1_1	Gain	expr	ymax(dB20((VF("/output") / VF("/i...))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>
amplifier_common_source_testbench_1_1	Bandwidth	expr	bandwidth((VF("/output") / VF("/i...))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>
amplifier_common_source_testbench_1_1	Current Consumption	expr	mag(IDC("/V0/PLUS"))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>
amplifier_common_source_testbench_1_1	Power Consumption	expr	mag((IDC("/V0/PLUS") * VDC("/n...))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>

mouse L: M: R:

2(5) Create Spec Comparison

## 2. Testbench Modification (*continued*)

- Select the test “amplifier\_common\_source\_testbench\_1” and left-click once to rename it to “testbench\_pre\_layout”.
- Select the test “amplifier\_common\_source\_testbench\_1\_1” and left-click once to rename it to “testbench\_post\_layout”.
- Note that if by mistake you switched to ADE Explorer, click on the blue arrow to switch back to ADE Assembler. Also, make sure to check the Global Variables.

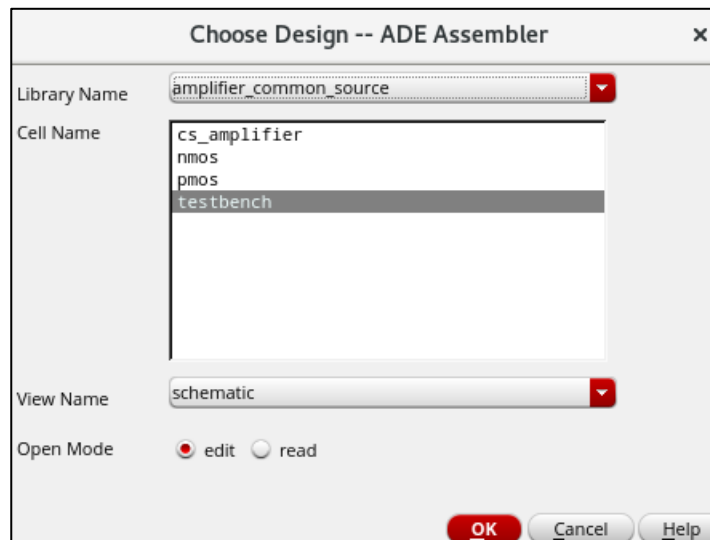
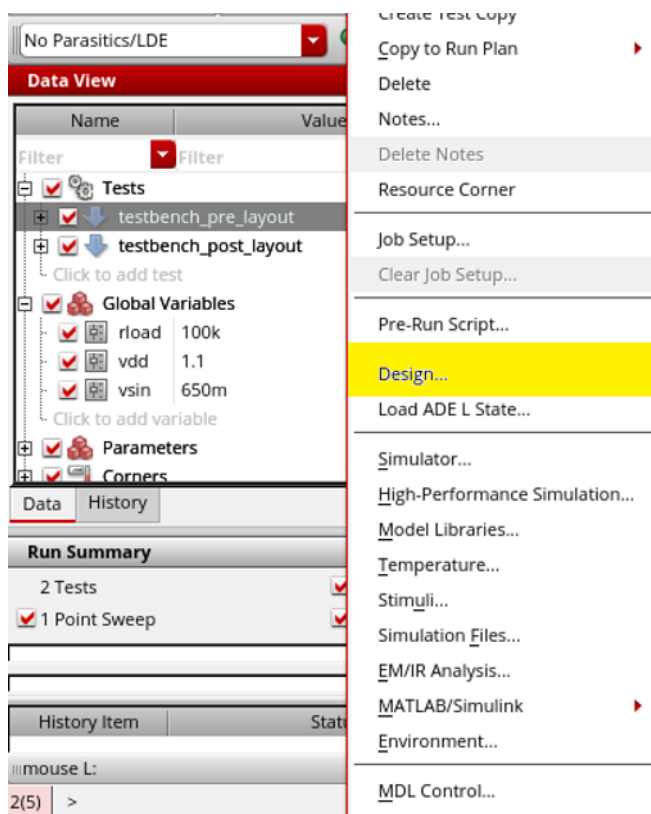


The screenshot shows the Virtuoso ADE Assembler interface. The left pane displays a tree view with 'Tests' containing 'testbench\_pre\_layout' and 'testbench\_post\_layout', and 'Global Variables' containing 'rload', 'vdd', and 'vsin'. The right pane shows a table of test results.

Test	Name	Type	Details	EvalType	Plot	Save	Spec
testbench_pre_layout	/input	signal		point			
testbench_pre_layout	/output	signal		point			
testbench_pre_layout	Gain	expr	$\text{ymax}(\text{dB20}((\text{VF}"/\text{output}")) / \text{VF}"/\dots)$	point	<input checked="" type="checkbox"/>		> 7.5
testbench_pre_layout	Bandwidth	expr	$\text{bandwidth}((\text{VF}"/\text{output}")) / \text{VF}"/\dots)$	point	<input checked="" type="checkbox"/>		> 4G
testbench_pre_layout	Current Consumption	expr	$\text{mag}(\text{IDC}"/\text{V0}/\text{PLUS}"))$	point	<input checked="" type="checkbox"/>		< 2.5m
testbench_pre_layout	Power Consumption	expr	$\text{mag}(\text{IDC}"/\text{V0}/\text{PLUS}")) * \text{VDC}"/\text{n}...$	point	<input checked="" type="checkbox"/>		< 2.75m
testbench_post_layout	/input	signal		point			
testbench_post_layout	/output	signal		point			
testbench_post_layout	Gain	expr	$\text{ymax}(\text{dB20}((\text{VF}"/\text{output}")) / \text{VF}"/\dots)$	point	<input checked="" type="checkbox"/>		> 7.5
testbench_post_layout	Bandwidth	expr	$\text{bandwidth}((\text{VF}"/\text{output}")) / \text{VF}"/\dots)$	point	<input checked="" type="checkbox"/>		> 4G
testbench_post_layout	Current Consumption	expr	$\text{mag}(\text{IDC}"/\text{V0}/\text{PLUS}"))$	point	<input checked="" type="checkbox"/>		< 2.5m
testbench_post_layout	Power Consumption	expr	$\text{mag}(\text{IDC}"/\text{V0}/\text{PLUS}")) * \text{VDC}"/\text{n}...$	point	<input checked="" type="checkbox"/>		< 2.75m

## 2. Testbench Modification (*continued*)

- Select the test “**testbench\_pre\_layout**”, right-click and select Design.
- The Choose Design – ADE Assembler form opens.
- Make sure the View Name is set to **schematic**. Click OK.
- Select the test again, right-click and select Model Libraries. Make sure the “**gpdk045.scs**” file is selected, and the **section** is set to **tt**.

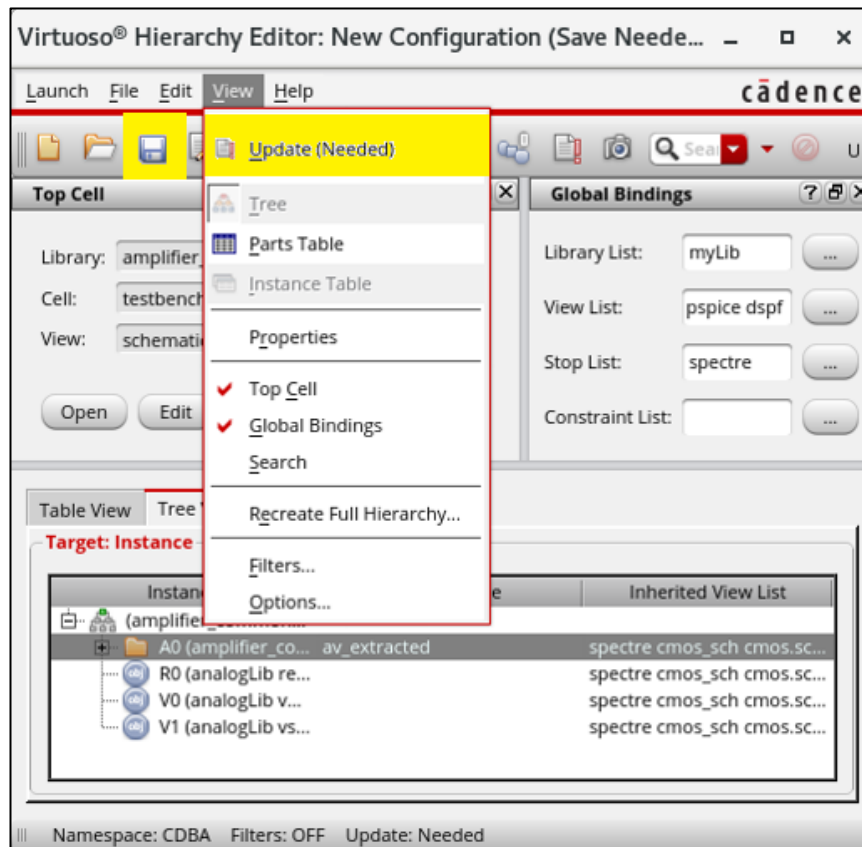


- Note that if the Model Libraries are not defined, please check Module 3 slide 14.



## 2. Testbench Modification (*continued*)

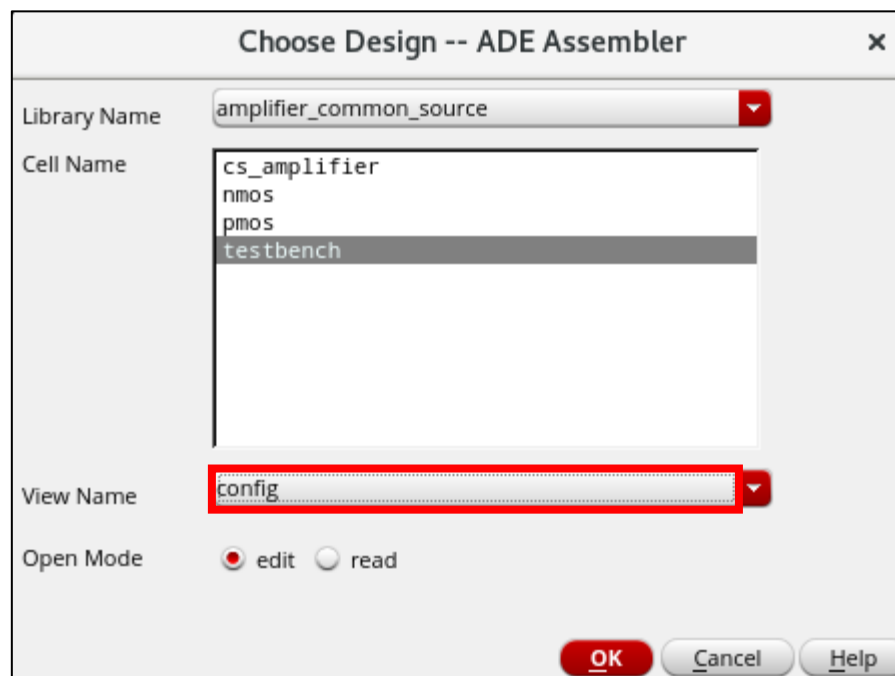
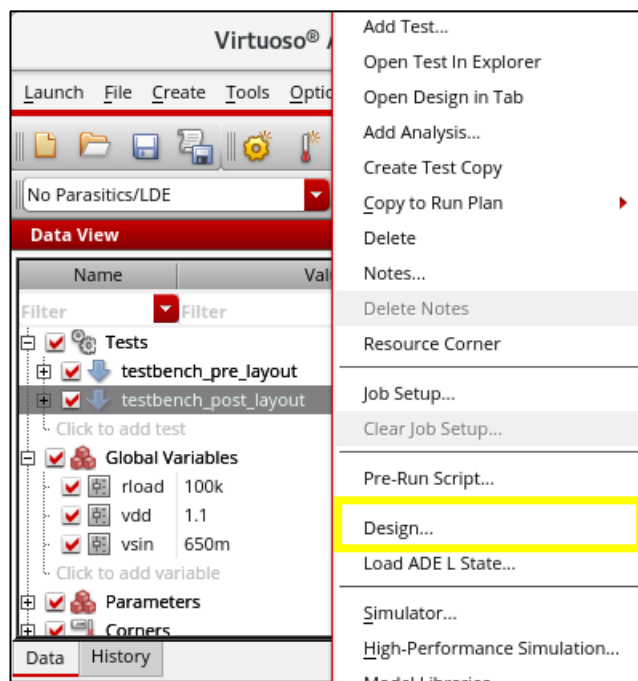
- From the taskbar, open the Virtuoso Hierarchy Editor.
- Click on View → Update (Needed) and save the config file.



- Note that we need to update and save the config file when we make modifications.

## 2. Testbench Modification (*continued*)

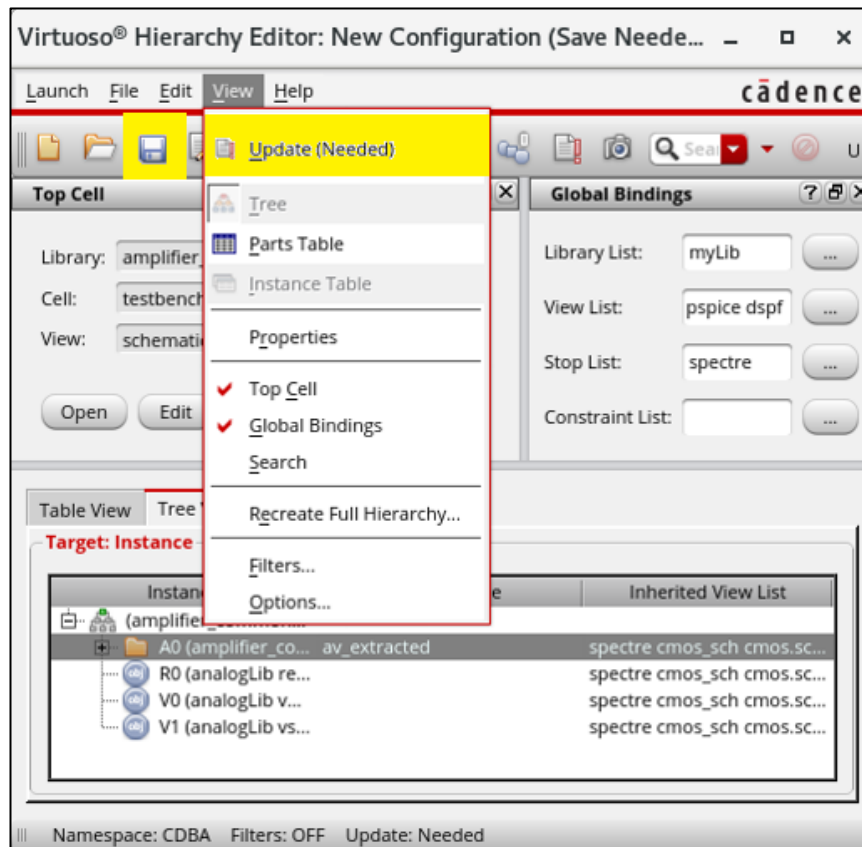
- Select the test “**testbench\_post\_layout**”, right-click and select Design.
- The Choose Design – ADE Assembler form opens.
- Change the View Name to **config**.
- Select the test again, right-click and select Model Libraries. Make sure the “**gpdk045.scs**” file is selected, and the **section** is set to **tt**.



- Since the av\_extracted file was set in the config file, we choose the View Name “config” for the post-layout simulations.
- Note that if the Model Libraries are not defined, please check Module 3 slide 14.

## 2. Testbench Modification (*continued*)

- From the taskbar, open the Virtuoso Hierarchy Editor.
- Click on View → Update (Needed) and save the config file.

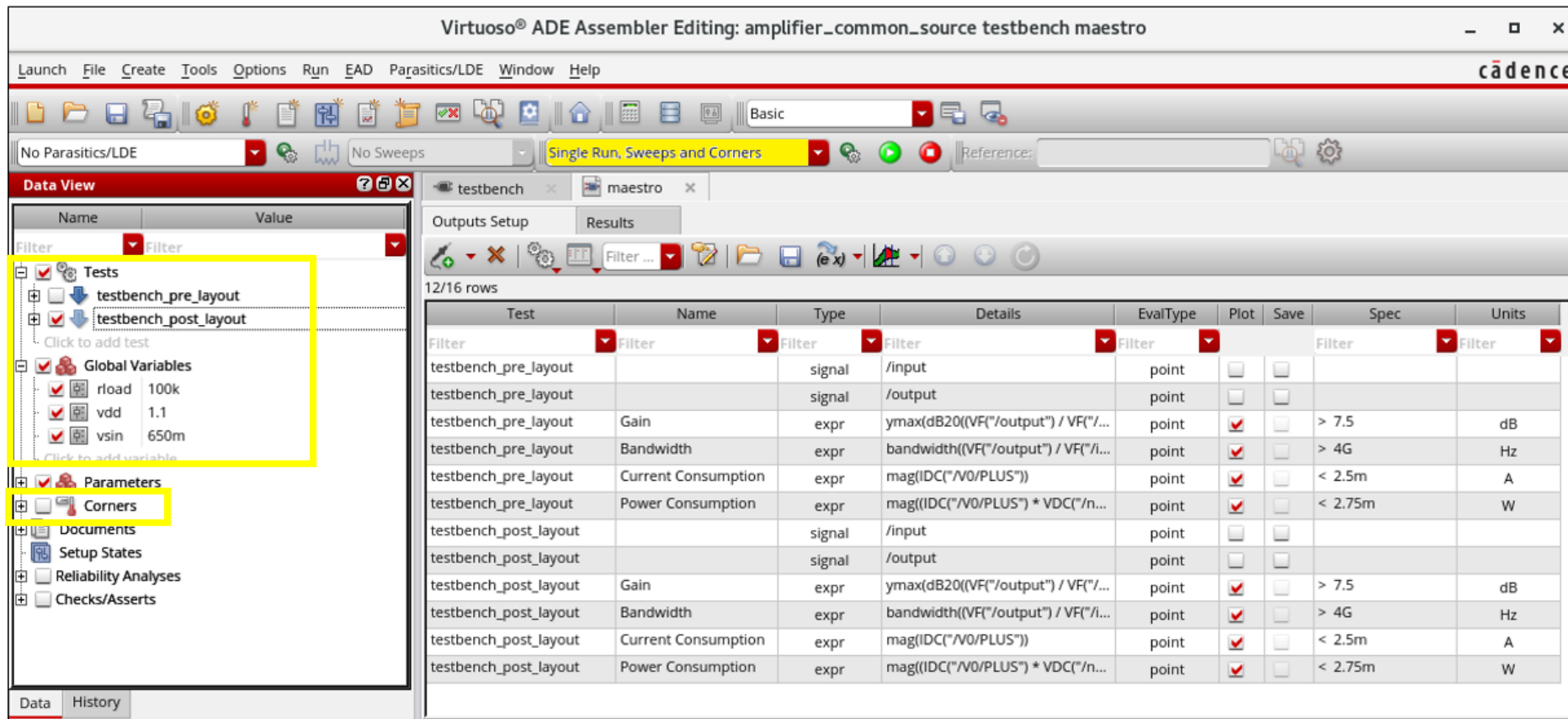


- Note that we need to update and save the config file when we make modifications.

## 3. DC and AC Analysis

### 3. DC and AC Analysis

- Uncheck the test “**testbench\_pre\_layout**”, since we want to run the analyses only for the post-layout now.
- Make sure the test “**testbench\_post\_layout**” is enabled.
- Uncheck Corners, and select Single Run, Sweeps and Corners from the drop-down list.
- Make sure to uncheck **Enable Electrical data Capture from EAD Flow** in EAD → setup...

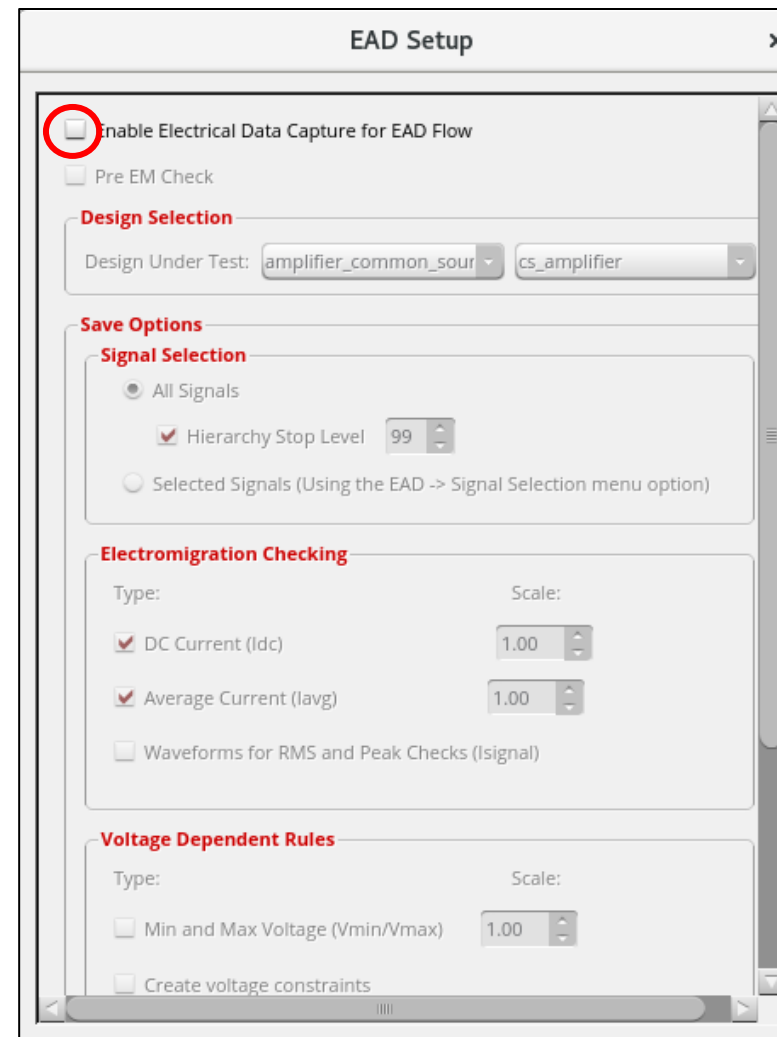
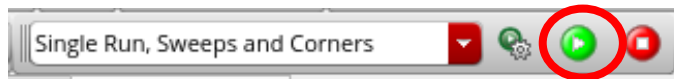


The screenshot shows the Cadence Virtuoso ADE Assembler Editing window for a testbench named 'maestro'. The 'Data View' pane on the left shows the testbench configuration. The 'Tests' section is expanded, showing 'testbench\_pre\_layout' and 'testbench\_post\_layout'. The 'testbench\_pre\_layout' test is unchecked, while 'testbench\_post\_layout' is checked. The 'Global Variables' section shows 'rload' set to 100k, 'vdd' set to 1.1, and 'vsin' set to 650m. The 'Parameters' section is also expanded. The 'Corners' section is highlighted with a yellow box. The 'Outputs Setup' pane on the right shows a table of test results.

Test	Name	Type	Details	EvalType	Plot	Save	Spec	Units
testbench_pre_layout	/input	signal		point	<input type="checkbox"/>	<input type="checkbox"/>		
testbench_pre_layout	/output	signal		point	<input type="checkbox"/>	<input type="checkbox"/>		
testbench_pre_layout	Gain	expr	$\text{ymax}(\text{dB20}((\text{VF}("/\text{output}")) / \text{VF}("/\text{input}")))$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 7.5	dB
testbench_pre_layout	Bandwidth	expr	$\text{bandwidth}((\text{VF}("/\text{output}")) / \text{VF}("/\text{input}"))$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 4G	Hz
testbench_pre_layout	Current Consumption	expr	$\text{mag}(\text{IDC}("/\text{V0/PLUS}"))$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	< 2.5m	A
testbench_pre_layout	Power Consumption	expr	$\text{mag}((\text{IDC}("/\text{V0/PLUS}")) * \text{VDC}("/\text{n...}"))$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	< 2.75m	W
testbench_post_layout	/input	signal		point	<input type="checkbox"/>	<input type="checkbox"/>		
testbench_post_layout	/output	signal		point	<input type="checkbox"/>	<input type="checkbox"/>		
testbench_post_layout	Gain	expr	$\text{ymax}(\text{dB20}((\text{VF}("/\text{output}")) / \text{VF}("/\text{input}")))$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 7.5	dB
testbench_post_layout	Bandwidth	expr	$\text{bandwidth}((\text{VF}("/\text{output}")) / \text{VF}("/\text{input}"))$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 4G	Hz
testbench_post_layout	Current Consumption	expr	$\text{mag}(\text{IDC}("/\text{V0/PLUS}"))$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	< 2.5m	A
testbench_post_layout	Power Consumption	expr	$\text{mag}((\text{IDC}("/\text{V0/PLUS}")) * \text{VDC}("/\text{n...}"))$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	< 2.75m	W

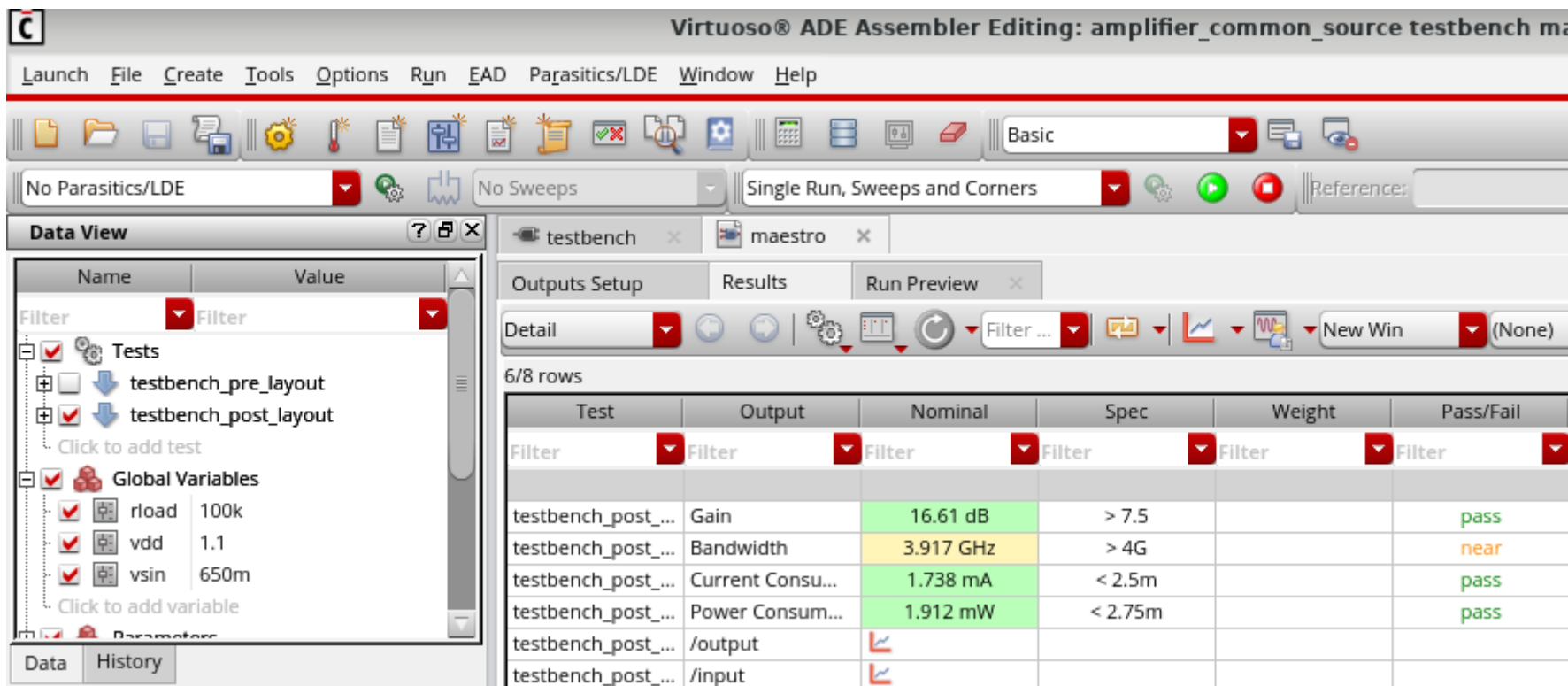
### 3. DC and AC Analysis

- EAD setup should look like this before running the simulation.
- Press on OK to close EAD Setup.
- Run the simulation.



### 3. DC and AC Analysis (*continued*)

- ADE Assembler automatically switches to the Results tab.
- The results are shown below.

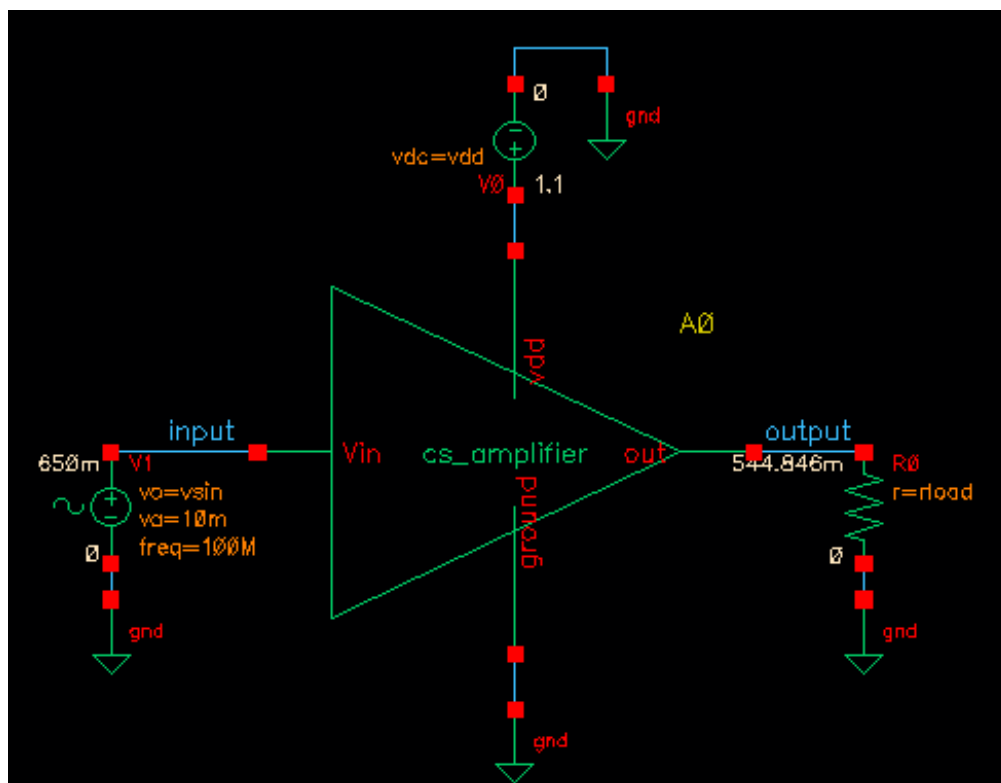


The screenshot shows the Virtuoso ADE Assembler interface with the Results tab selected. The left pane displays the testbench configuration, including tests and global variables. The right pane shows a table of test results for 6/8 rows.

Test	Output	Nominal	Spec	Weight	Pass/Fail
testbench_post_...	Gain	16.61 dB	> 7.5		pass
testbench_post_...	Bandwidth	3.917 GHz	> 4G		near
testbench_post_...	Current Consum...	1.738 mA	< 2.5m		pass
testbench_post_...	Power Consum...	1.912 mW	< 2.75m		pass
testbench_post_...	/output				
testbench_post_...	/input				

### 3. DC and AC Analysis (*continued*)

- To view the DC Node Voltages and Operating Points, from the **Results** tab, select any result and right-click → Results → Annotate → DC Node Voltages and DC Operating Points.
- ADE Assembler switches automatically to the testbench tab showing the DC Node Voltages and Operating Points.

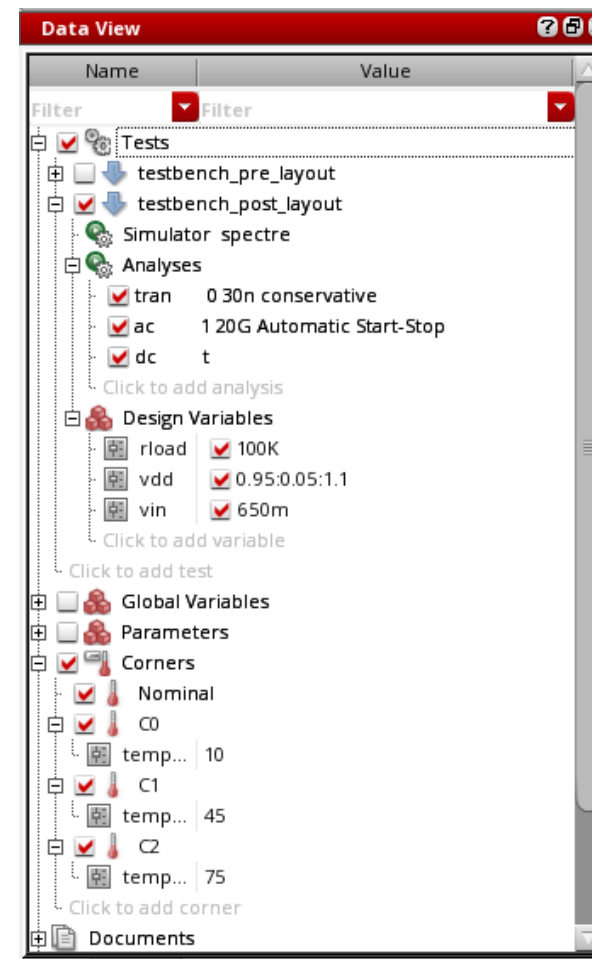




## 4. Measurements Across Sweeps and Corners

## 4. Measurements Across Sweeps and Corners

- To run the simulation across sweeps and corners, we have to define the sweeps and corners.
- Note since we are using a copy of the original testbench used in Module 4, the corners are set.
- Uncheck the Global Variables.
- Check the Corners.
- Expand the test “testbench\_post\_layout”, the Analysis, and the Design Variables.
- Make sure to have the setup as shown in the figure.
- Run the simulation.



## 4. Measurements Across Sweeps and Corners (continued)

- The results are displayed for the “tt” process corners.
- The gain is better for higher vdd values.
- The current and power consumption pass the given specs.
- As for the bandwidth, the parasitics have affected the results.

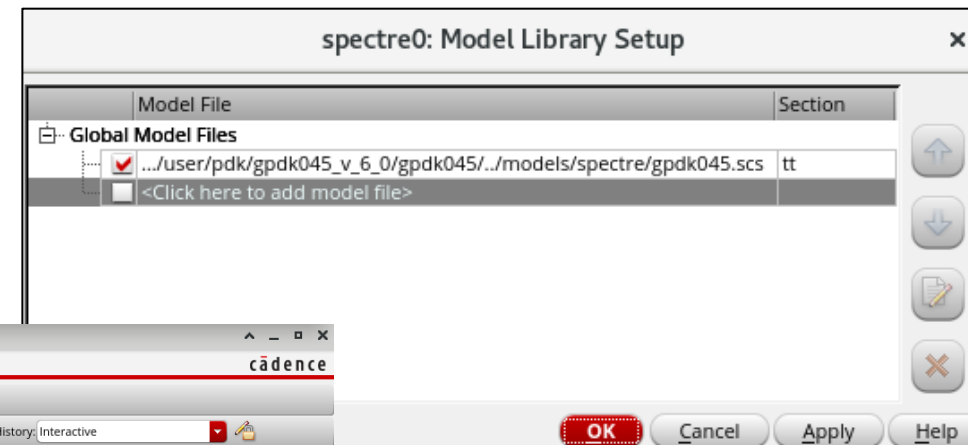
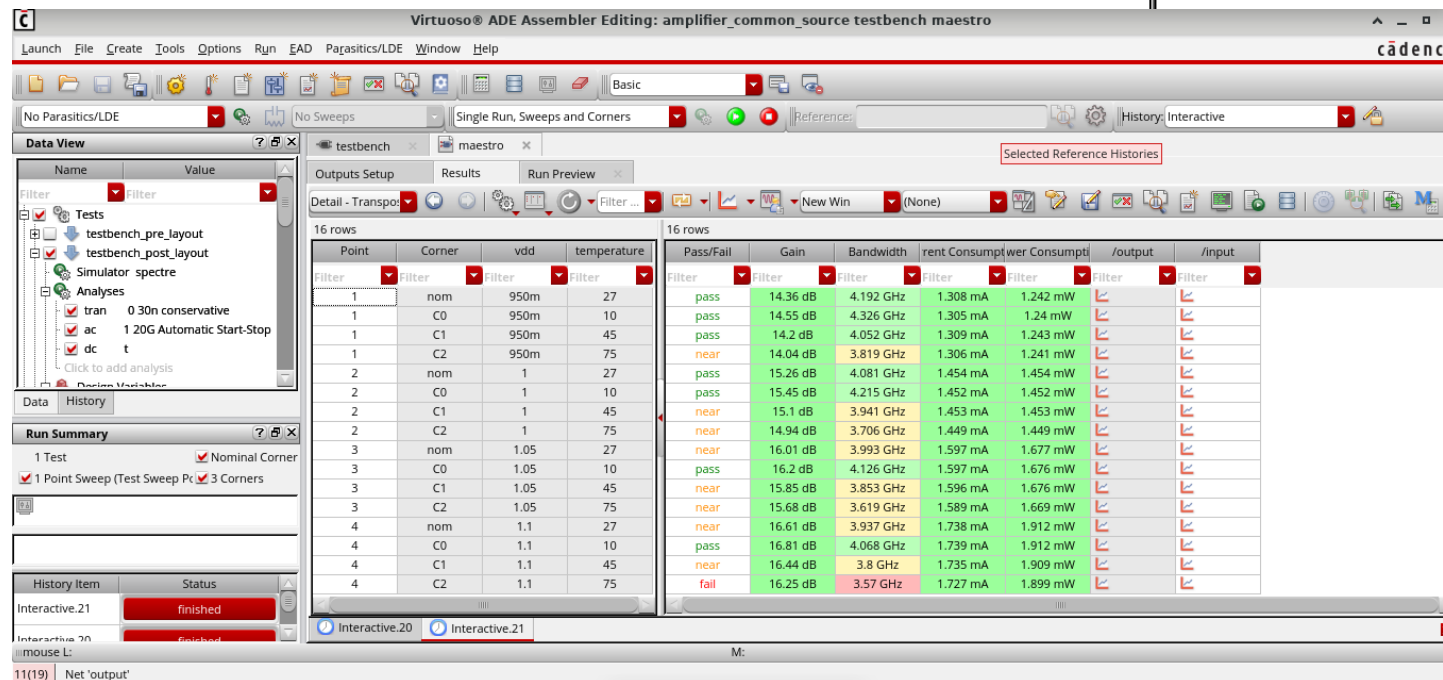
Configuration View

Testbench Modification

DC and AC Analysis

Measurements Across Sweeps and Corners

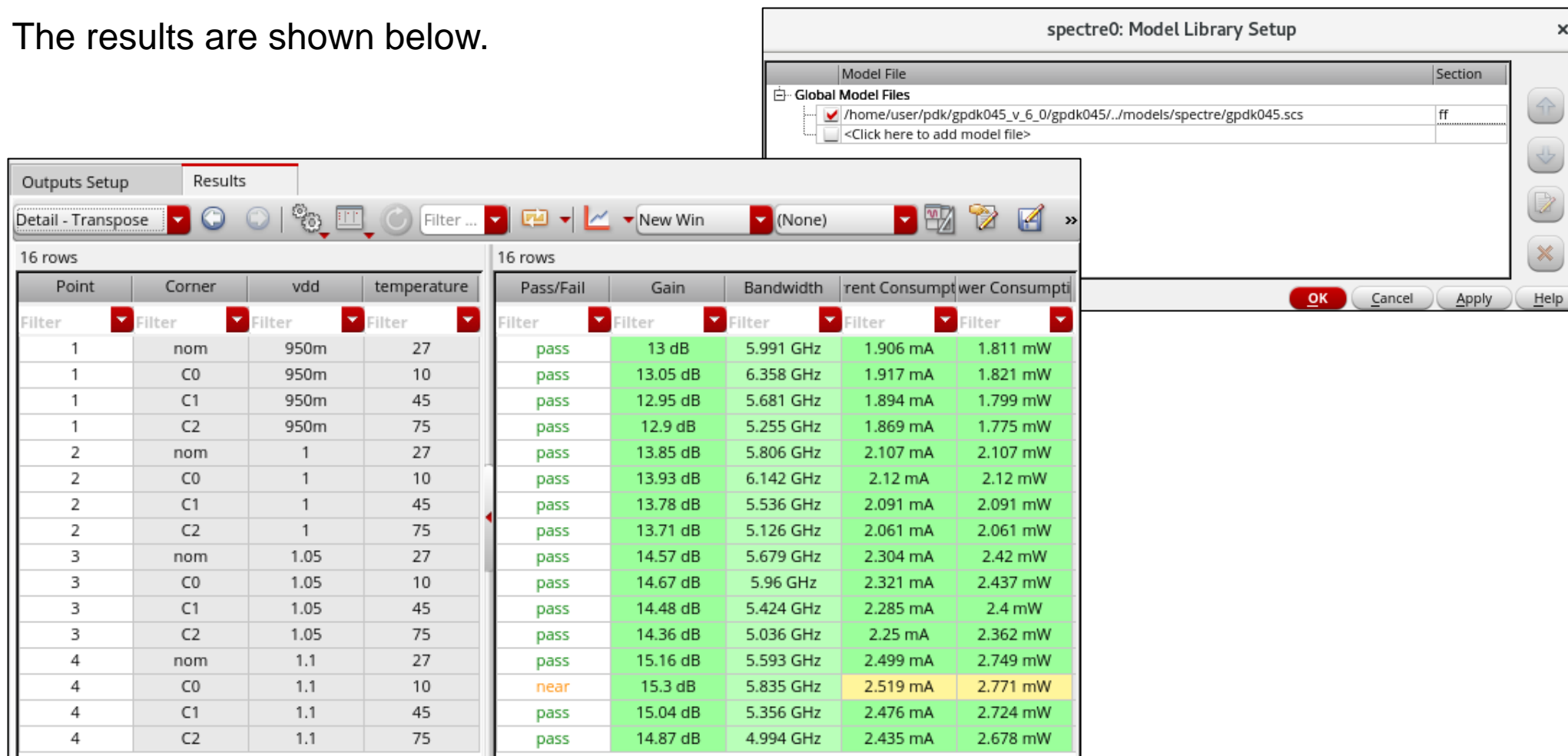
Monte Carlo Analysis

Point	Corner	vdd	temperature	Pass/Fail	Gain	Bandwidth	rent Consumpt	wer Consumpt	/output	/input
1	nom	950m	27	pass	14.36 dB	4.192 GHz	1.308 mA	1.242 mW		
1	C0	950m	10	pass	14.55 dB	4.326 GHz	1.305 mA	1.24 mW		
1	C1	950m	45	pass	14.2 dB	4.052 GHz	1.309 mA	1.243 mW		
1	C2	950m	75	near	14.04 dB	3.819 GHz	1.306 mA	1.241 mW		
2	nom	1	27	pass	15.26 dB	4.081 GHz	1.454 mA	1.454 mW		
2	C0	1	10	pass	15.45 dB	4.215 GHz	1.452 mA	1.452 mW		
2	C1	1	45	near	15.1 dB	3.941 GHz	1.453 mA	1.453 mW		
2	C2	1	75	near	14.94 dB	3.706 GHz	1.449 mA	1.449 mW		
3	nom	1.05	27	near	16.01 dB	3.993 GHz	1.597 mA	1.677 mW		
3	C0	1.05	10	pass	16.2 dB	4.126 GHz	1.597 mA	1.676 mW		
3	C1	1.05	45	near	15.85 dB	3.853 GHz	1.596 mA	1.676 mW		
3	C2	1.05	75	near	15.68 dB	3.619 GHz	1.589 mA	1.669 mW		
4	nom	1.1	27	near	16.61 dB	3.937 GHz	1.738 mA	1.912 mW		
4	C0	1.1	10	pass	16.81 dB	4.068 GHz	1.739 mA	1.912 mW		
4	C1	1.1	45	near	16.44 dB	3.8 GHz	1.735 mA	1.909 mW		
4	C2	1.1	75	fail	16.25 dB	3.57 GHz	1.727 mA	1.899 mW		

## 4. Measurements Across Sweeps and Corners (continued)

- Select the test “testbench\_post\_layout” from the Data View. Right-click and select Model Libraries. Change the section to “ff” and run the simulation.
- The results are shown below.



The screenshot shows the 'spectre0: Model Library Setup' dialog box and the 'Results' window. The dialog box shows the 'Model File' as '/home/user/pdk/gpdk045\_v\_6\_0/gpdk045/.../models/spectre/gpdk045.scs' and the 'Section' as 'ff'. The 'Results' window displays two tables of simulation results.

**Table 1: Simulation Parameters**

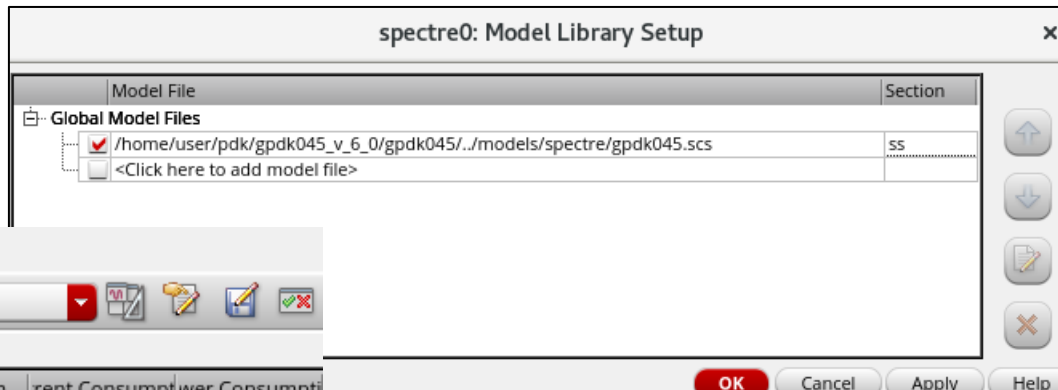
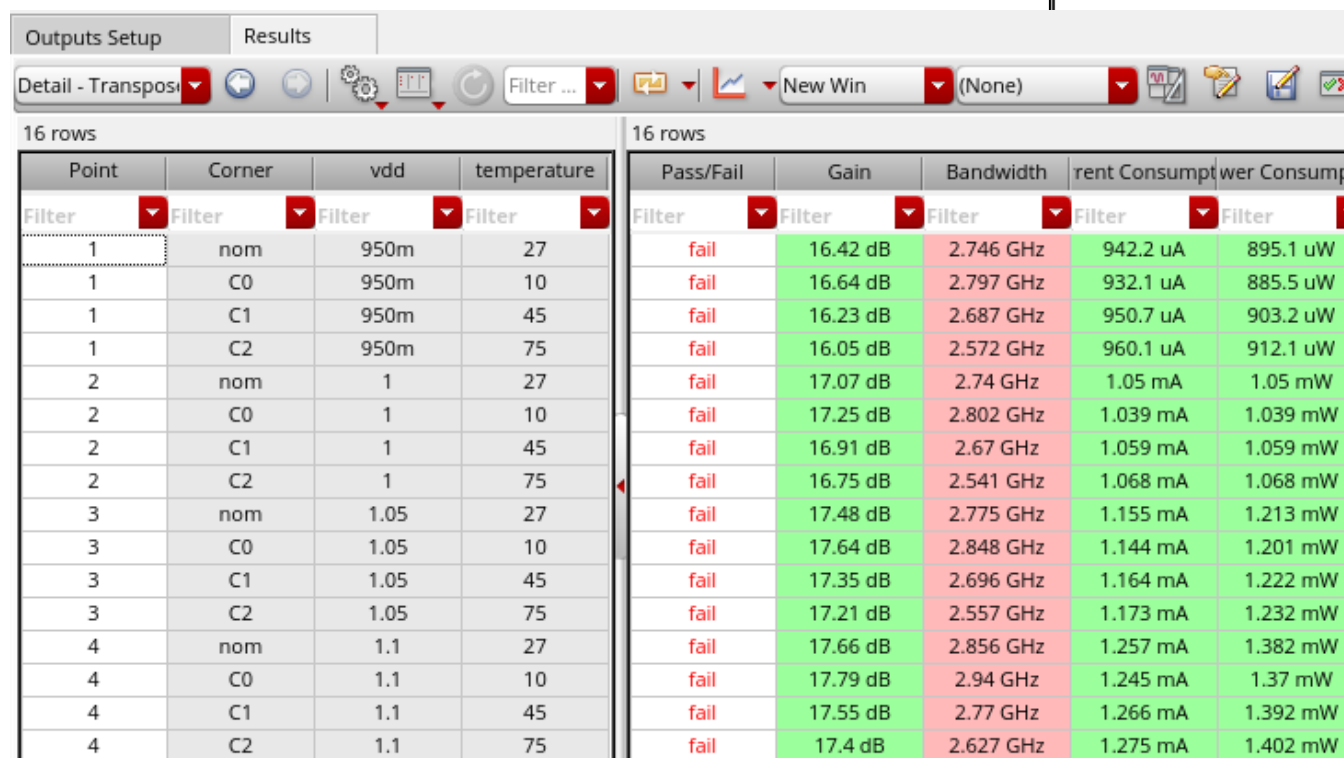
Point	Corner	vdd	temperature
1	nom	950m	27
1	C0	950m	10
1	C1	950m	45
1	C2	950m	75
2	nom	1	27
2	C0	1	10
2	C1	1	45
2	C2	1	75
3	nom	1.05	27
3	C0	1.05	10
3	C1	1.05	45
3	C2	1.05	75
4	nom	1.1	27
4	C0	1.1	10
4	C1	1.1	45
4	C2	1.1	75

**Table 2: Simulation Results**

Pass/Fail	Gain	Bandwidth	rent Consumpt	wer Consumpt
pass	13 dB	5.991 GHz	1.906 mA	1.811 mW
pass	13.05 dB	6.358 GHz	1.917 mA	1.821 mW
pass	12.95 dB	5.681 GHz	1.894 mA	1.799 mW
pass	12.9 dB	5.255 GHz	1.869 mA	1.775 mW
pass	13.85 dB	5.806 GHz	2.107 mA	2.107 mW
pass	13.93 dB	6.142 GHz	2.12 mA	2.12 mW
pass	13.78 dB	5.536 GHz	2.091 mA	2.091 mW
pass	13.71 dB	5.126 GHz	2.061 mA	2.061 mW
pass	14.57 dB	5.679 GHz	2.304 mA	2.42 mW
pass	14.67 dB	5.96 GHz	2.321 mA	2.437 mW
pass	14.48 dB	5.424 GHz	2.285 mA	2.4 mW
pass	14.36 dB	5.036 GHz	2.25 mA	2.362 mW
pass	15.16 dB	5.593 GHz	2.499 mA	2.749 mW
near	15.3 dB	5.835 GHz	2.519 mA	2.771 mW
pass	15.04 dB	5.356 GHz	2.476 mA	2.724 mW
pass	14.87 dB	4.994 GHz	2.435 mA	2.678 mW

## 4. Measurements Across Sweeps and Corners (continued)

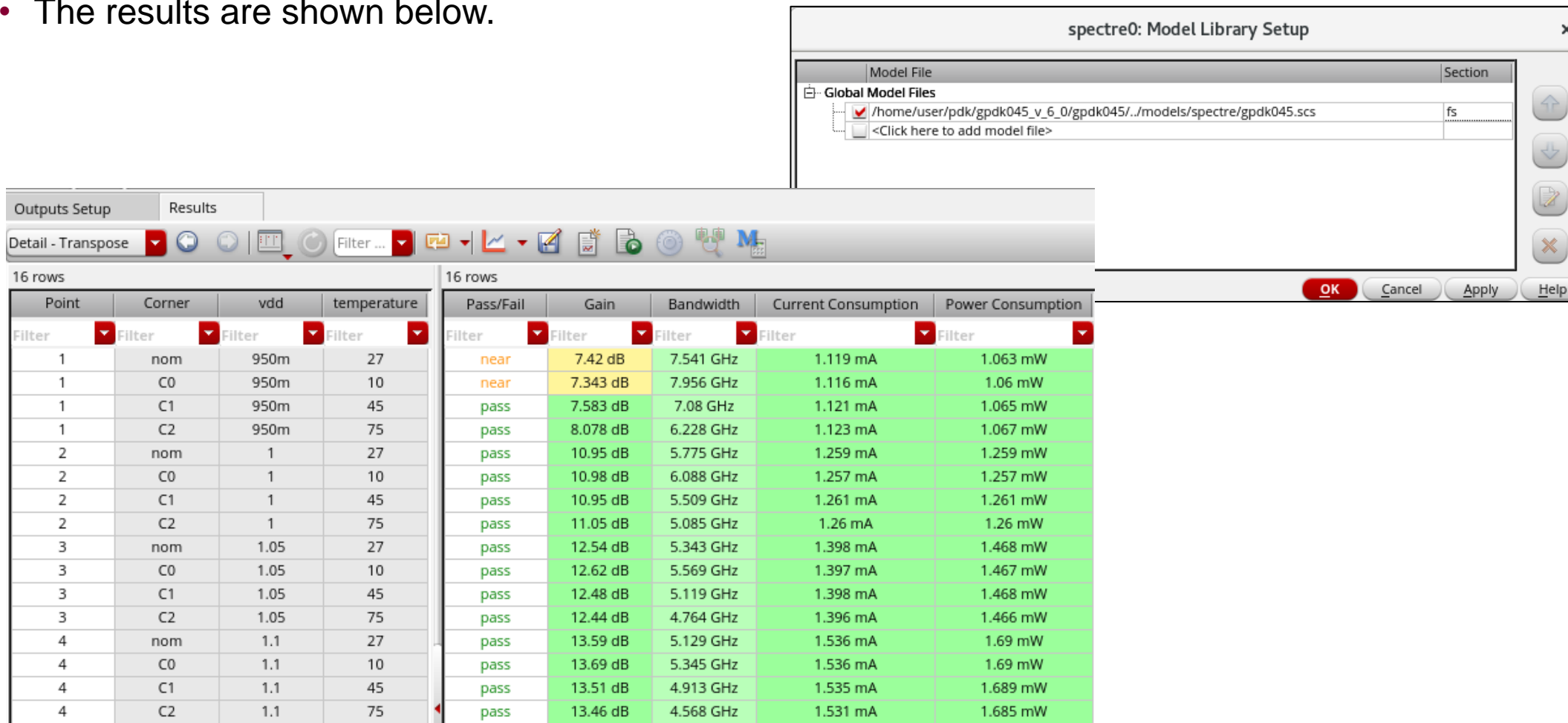
- Select the test “testbench\_post\_layout” from the Data View. Right-click and select Model Libraries. Change the section to “ss” and run the simulation.
- The bandwidth fails in all cases.
- The results are shown below.

Point	Corner	vdd	temperature	Pass/Fail	Gain	Bandwidth	rent Consumpt	power Consumpt
1	nom	950m	27	fail	16.42 dB	2.746 GHz	942.2 uA	895.1 uW
1	C0	950m	10	fail	16.64 dB	2.797 GHz	932.1 uA	885.5 uW
1	C1	950m	45	fail	16.23 dB	2.687 GHz	950.7 uA	903.2 uW
1	C2	950m	75	fail	16.05 dB	2.572 GHz	960.1 uA	912.1 uW
2	nom	1	27	fail	17.07 dB	2.74 GHz	1.05 mA	1.05 mW
2	C0	1	10	fail	17.25 dB	2.802 GHz	1.039 mA	1.039 mW
2	C1	1	45	fail	16.91 dB	2.67 GHz	1.059 mA	1.059 mW
2	C2	1	75	fail	16.75 dB	2.541 GHz	1.068 mA	1.068 mW
3	nom	1.05	27	fail	17.48 dB	2.775 GHz	1.155 mA	1.213 mW
3	C0	1.05	10	fail	17.64 dB	2.848 GHz	1.144 mA	1.201 mW
3	C1	1.05	45	fail	17.35 dB	2.696 GHz	1.164 mA	1.222 mW
3	C2	1.05	75	fail	17.21 dB	2.557 GHz	1.173 mA	1.232 mW
4	nom	1.1	27	fail	17.66 dB	2.856 GHz	1.257 mA	1.382 mW
4	C0	1.1	10	fail	17.79 dB	2.94 GHz	1.245 mA	1.37 mW
4	C1	1.1	45	fail	17.55 dB	2.77 GHz	1.266 mA	1.392 mW
4	C2	1.1	75	fail	17.4 dB	2.627 GHz	1.275 mA	1.402 mW

## 4. Measurements Across Sweeps and Corners (continued)

- Change the section to “fs” and run the simulation.
- The results are shown below.



The screenshot displays the 'spectre0: Model Library Setup' dialog box and the 'Results' tab of the simulation output.

**Model Library Setup Dialog:**

Model File	Section
/home/user/pdk/gpdk045_v_6_0/gpdk045/./models/spectre/gpdk045.scs	fs
<Click here to add model file>	

**Simulation Results (Results Tab):**

16 rows

Point	Corner	vdd	temperature
1	nom	950m	27
1	C0	950m	10
1	C1	950m	45
1	C2	950m	75
2	nom	1	27
2	C0	1	10
2	C1	1	45
2	C2	1	75
3	nom	1.05	27
3	C0	1.05	10
3	C1	1.05	45
3	C2	1.05	75
4	nom	1.1	27
4	C0	1.1	10
4	C1	1.1	45
4	C2	1.1	75

16 rows

Pass/Fail	Gain	Bandwidth	Current Consumption	Power Consumption
near	7.42 dB	7.541 GHz	1.119 mA	1.063 mW
near	7.343 dB	7.956 GHz	1.116 mA	1.06 mW
pass	7.583 dB	7.08 GHz	1.121 mA	1.065 mW
pass	8.078 dB	6.228 GHz	1.123 mA	1.067 mW
pass	10.95 dB	5.775 GHz	1.259 mA	1.259 mW
pass	10.98 dB	6.088 GHz	1.257 mA	1.257 mW
pass	10.95 dB	5.509 GHz	1.261 mA	1.261 mW
pass	11.05 dB	5.085 GHz	1.26 mA	1.26 mW
pass	12.54 dB	5.343 GHz	1.398 mA	1.468 mW
pass	12.62 dB	5.569 GHz	1.397 mA	1.467 mW
pass	12.48 dB	5.119 GHz	1.398 mA	1.468 mW
pass	12.44 dB	4.764 GHz	1.396 mA	1.466 mW
pass	13.59 dB	5.129 GHz	1.536 mA	1.69 mW
pass	13.69 dB	5.345 GHz	1.536 mA	1.69 mW
pass	13.51 dB	4.913 GHz	1.535 mA	1.689 mW
pass	13.46 dB	4.568 GHz	1.531 mA	1.685 mW

## 4. Measurements Across Sweeps and Corners (*continued*)

- Change the section to “**sf**” and run the simulation.
- In this case, the bandwidth fails for all the design points.
- The gain, current, and power consumption pass the given spec for all the design points.
- The results are shown below.

Configuration View  
↓  
Testbench Modification  
↓  
DC and AC Analysis  
↓  
**Measurements Across Sweeps and Corners**  
↓  
Monte Carlo Analysis

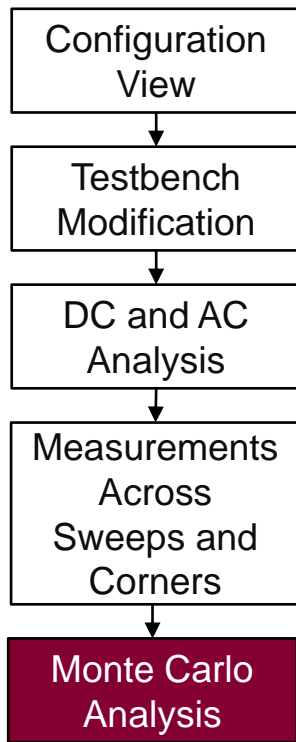
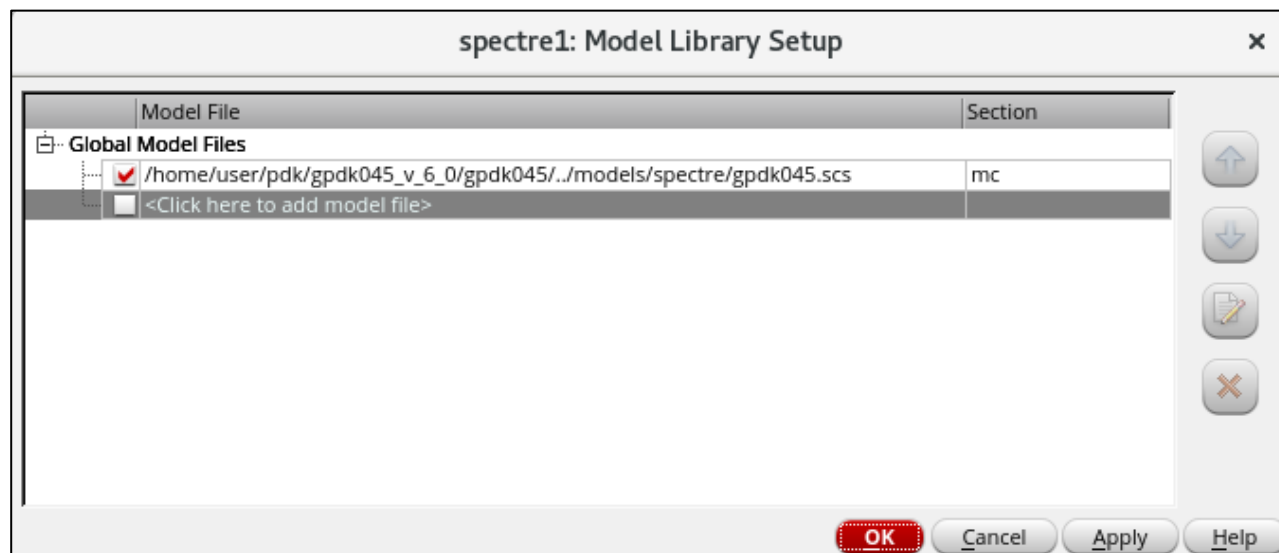
Point	Corner	vdd	temperature	Pass/Fail	Gain	Bandwidth	Current Consumption	Power Consumption
1	nom	950m	27	fail	15.6 dB	3.425 GHz	1.146 mA	1.089 mW
1	C0	950m	10	fail	15.8 dB	3.513 GHz	1.14 mA	1.083 mW
1	C1	950m	45	fail	15.43 dB	3.33 GHz	1.151 mA	1.093 mW
1	C2	950m	75	fail	15.26 dB	3.165 GHz	1.154 mA	1.096 mW
2	nom	1	27	fail	16.22 dB	3.404 GHz	1.261 mA	1.261 mW
2	C0	1	10	fail	16.42 dB	3.497 GHz	1.256 mA	1.256 mW
2	C1	1	45	fail	16.06 dB	3.305 GHz	1.266 mA	1.266 mW
2	C2	1	75	fail	15.89 dB	3.136 GHz	1.268 mA	1.268 mW
3	nom	1.05	27	fail	16.69 dB	3.412 GHz	1.375 mA	1.443 mW
3	C0	1.05	10	fail	16.88 dB	3.51 GHz	1.369 mA	1.438 mW
3	C1	1.05	45	fail	16.53 dB	3.309 GHz	1.378 mA	1.447 mW
3	C2	1.05	75	fail	16.36 dB	3.138 GHz	1.38 mA	1.449 mW
4	nom	1.1	27	fail	17 dB	3.453 GHz	1.485 mA	1.634 mW
4	C0	1.1	10	fail	17.19 dB	3.555 GHz	1.48 mA	1.628 mW
4	C1	1.1	45	fail	16.84 dB	3.348 GHz	1.489 mA	1.637 mW
4	C2	1.1	75	fail	16.65 dB	3.177 GHz	1.489 mA	1.638 mW

## 5. Monte Carlo Statistical Analysis



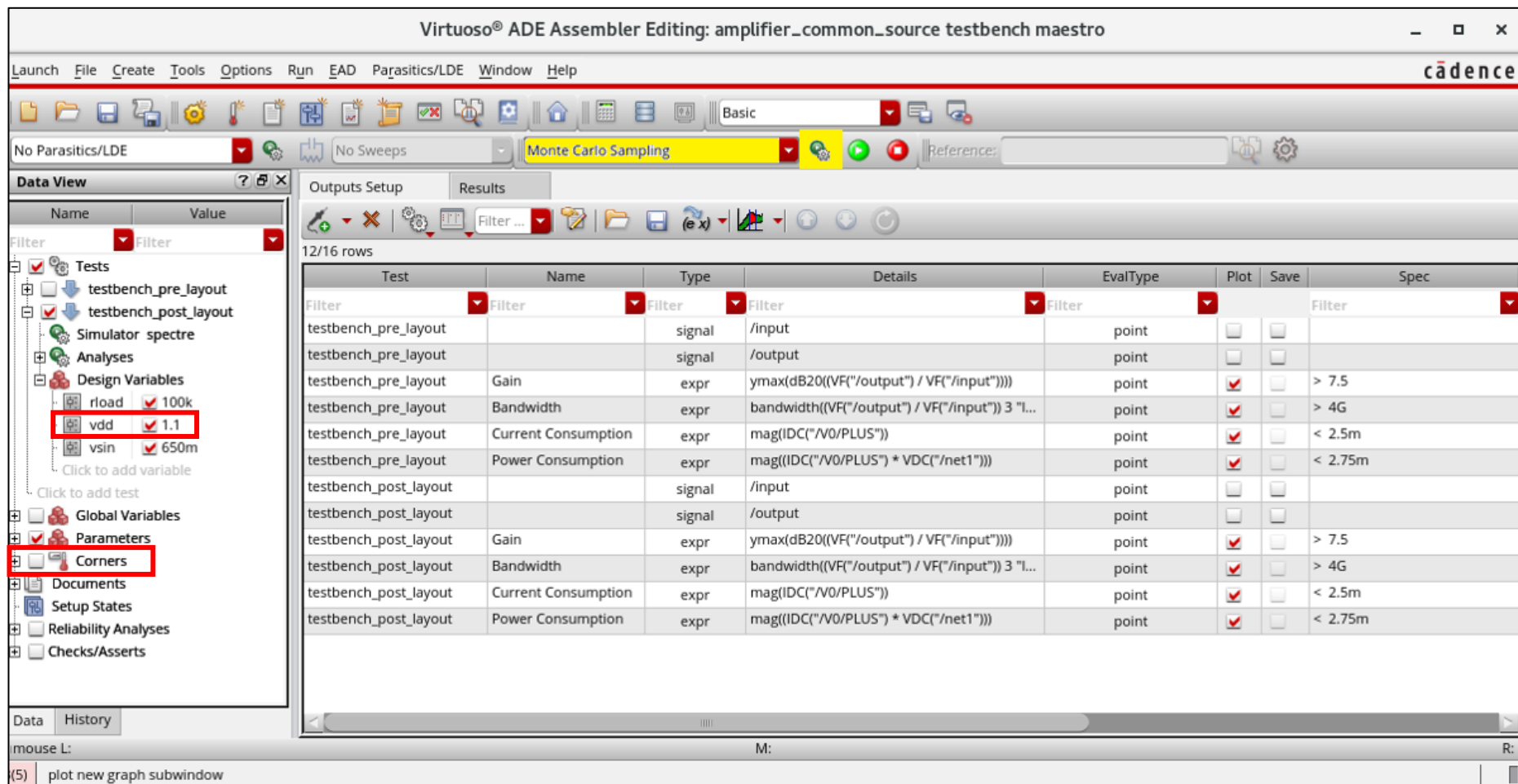
## 5. Monte Carlo Statistical Analysis

- Change the section to “**mc**”.



## 5. Monte Carlo Statistical Analysis


- To run the Monte Carlo Analysis, remove the sweep, uncheck Corners, and choose Monte Carlo Sampling from the drop-down list.

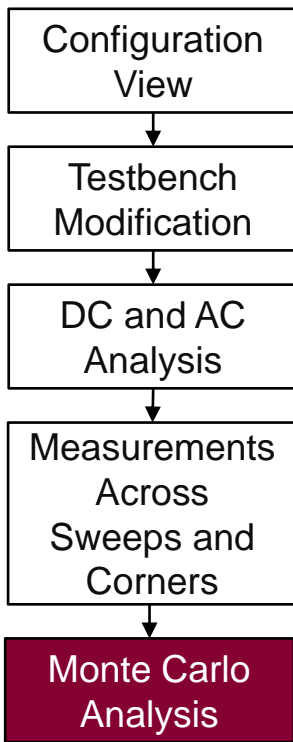
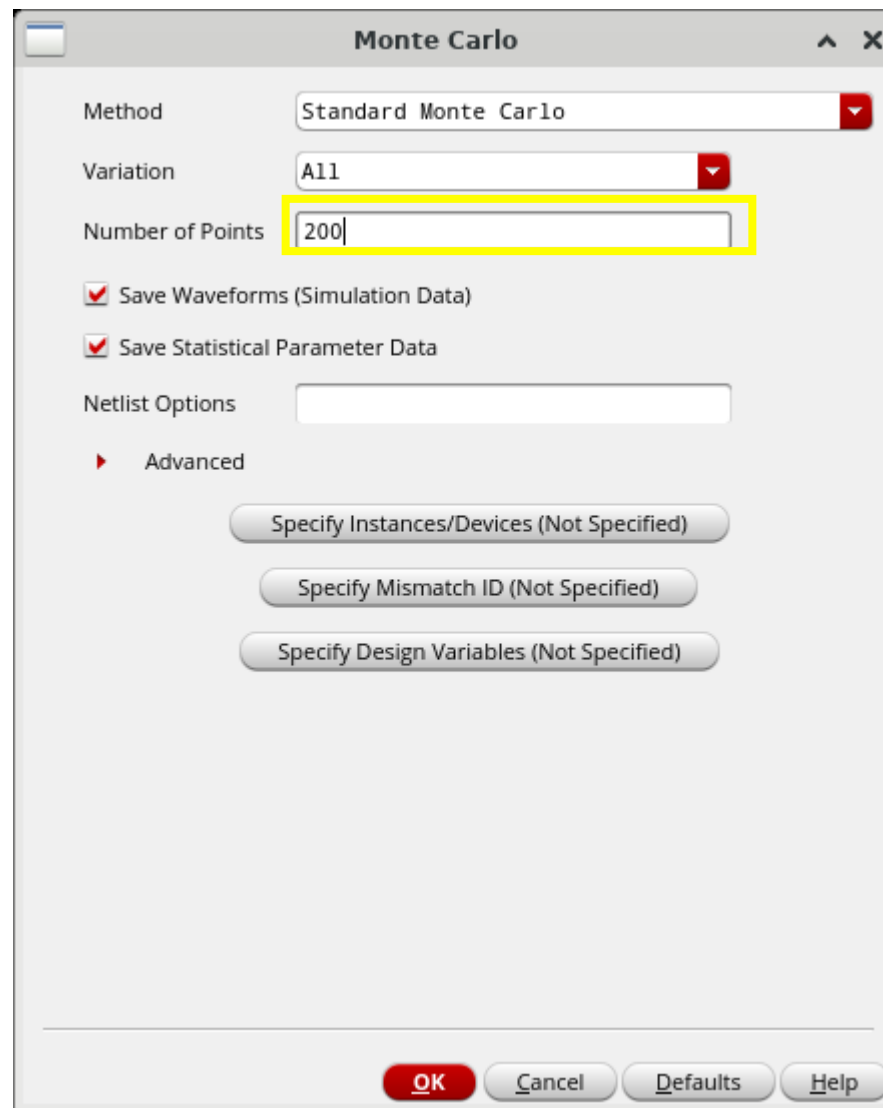


The screenshot shows the Cadence Virtuoso ADE Assembler interface for editing a testbench. The 'Launch' menu is open, and 'Monte Carlo Sampling' is selected. The 'Data View' pane on the left shows the 'Design Variables' section with 'vdd' set to 1.1 and 'vsin' set to 650m. The 'Corners' option is also visible. The 'Results' pane on the right shows a table of 12/16 rows, detailing the Monte Carlo sampling results for various testbench parameters.

Test	Name	Type	Details	EvalType	Plot	Save	Spec
testbench_pre_layout	/input	signal		point	<input type="checkbox"/>	<input type="checkbox"/>	
testbench_pre_layout	/output	signal		point	<input type="checkbox"/>	<input type="checkbox"/>	
testbench_pre_layout	Gain	expr	$\text{ymax}(\text{dB20}((\text{VF}("/\text{output"}) / \text{VF}("/\text{input}")))))$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 7.5
testbench_pre_layout	Bandwidth	expr	$\text{bandwidth}((\text{VF}("/\text{output"}) / \text{VF}("/\text{input}")) 3 "1...$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 4G
testbench_pre_layout	Current Consumption	expr	$\text{mag}(\text{IDC}("/\text{V0}/\text{PLUS}"))$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	< 2.5m
testbench_pre_layout	Power Consumption	expr	$\text{mag}((\text{IDC}("/\text{V0}/\text{PLUS}) * \text{VDC}("/\text{net1}")))$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	< 2.75m
testbench_post_layout	/input	signal		point	<input type="checkbox"/>	<input type="checkbox"/>	
testbench_post_layout	/output	signal		point	<input type="checkbox"/>	<input type="checkbox"/>	
testbench_post_layout	Gain	expr	$\text{ymax}(\text{dB20}((\text{VF}("/\text{output"}) / \text{VF}("/\text{input}")))))$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 7.5
testbench_post_layout	Bandwidth	expr	$\text{bandwidth}((\text{VF}("/\text{output"}) / \text{VF}("/\text{input}")) 3 "1...$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 4G
testbench_post_layout	Current Consumption	expr	$\text{mag}(\text{IDC}("/\text{V0}/\text{PLUS}"))$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	< 2.5m
testbench_post_layout	Power Consumption	expr	$\text{mag}((\text{IDC}("/\text{V0}/\text{PLUS}) * \text{VDC}("/\text{net1}")))$	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	< 2.75m

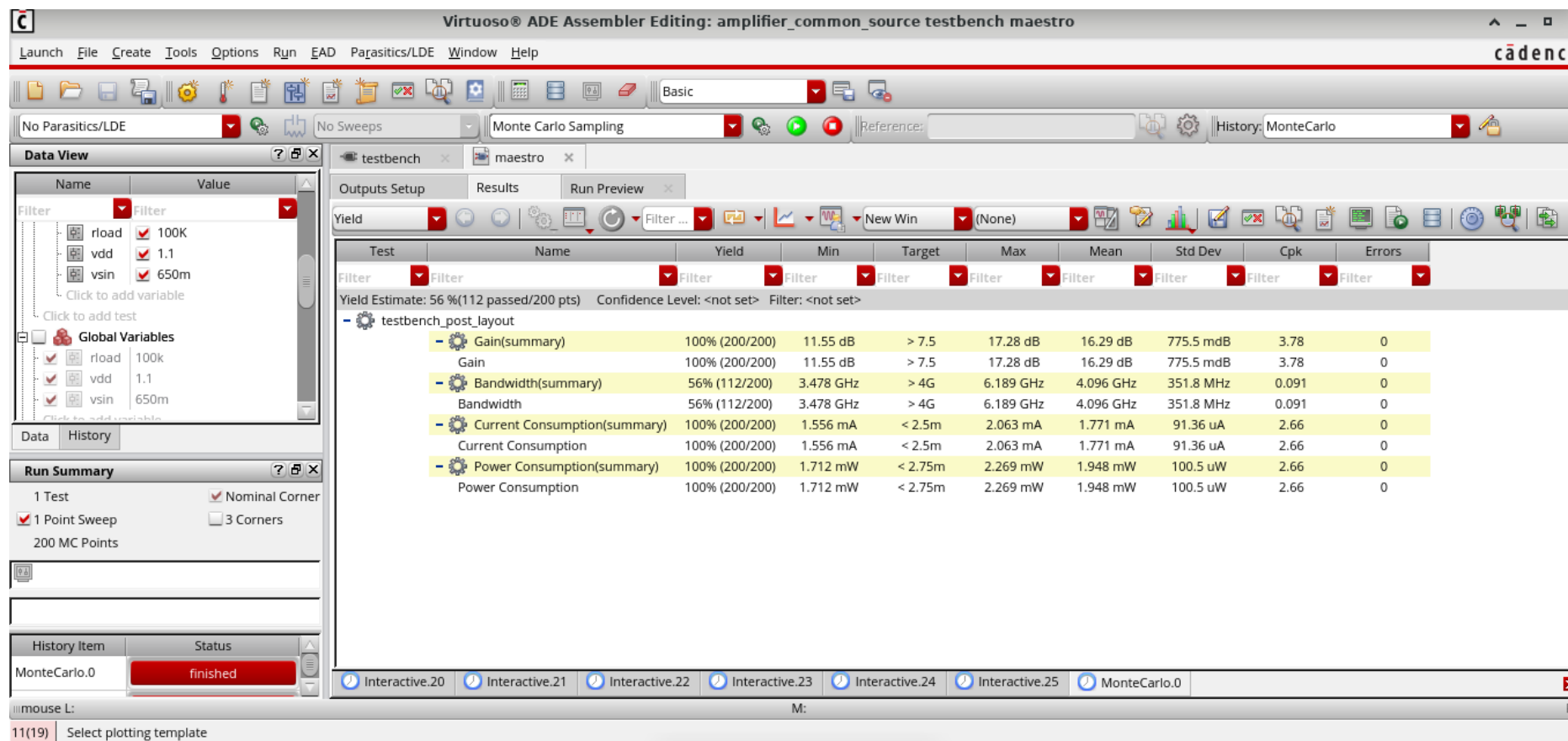
## 5. Monte Carlo Statistical Analysis (*continued*)

- Click on the Simulation Options button  and change the field “Run a fixed number of points” to 200.
- Run the simulation.



## 5. Monte Carlo Statistical Analysis (*continued*)

- The results are displayed using the “Yield” format, as shown below.



## 5. Monte Carlo Statistical Analysis (continued)

- Click on the icon  and select Plot All.
- The histograms plotted are shown below.

